MX Automotive Family FPGAs

FuseLock™

Features

- Single-Chip ASIC Alternative for Automotive Applications
- 3,000 to 54,000 System Gates
- Up to 2.5 kbits Configurable Dual-Port SRAM
- Fast Wide-Decode Circuitry
- Up to 202 User-Programmable I/O Pins

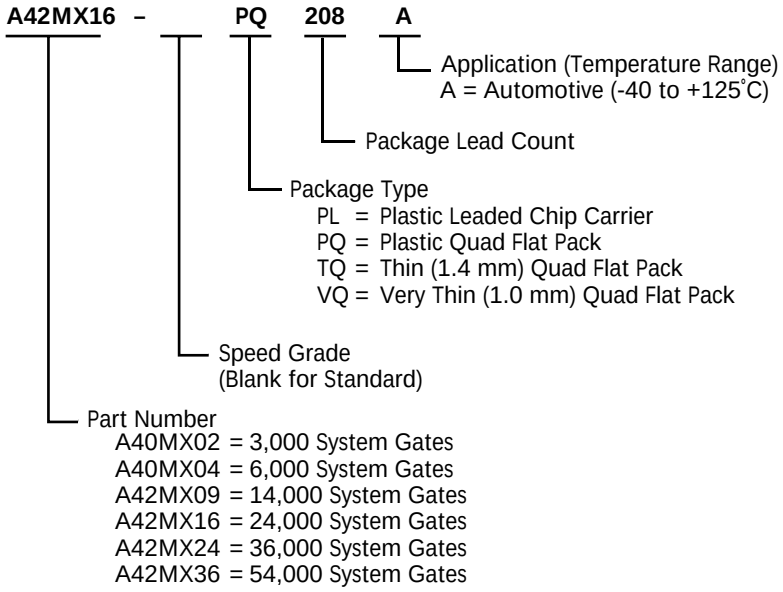
Ease of Integration

- Synthesis-Friendly Architecture Supports ASIC Design Methodologies
- Up to 100% Resource Utilization and 100% Pin Fixing
- Deterministic, User-Controllable Timing
- Unique In-System Diagnostic and Verification Capability with Silicon Explorer II
- Low Power Consumption
- IEEE Standard 1149.1 (JTAG) Boundary Scan Testing

Product Profile

Device	A40MX02	A40MX04	A42MX09	A42MX16	A42MX24	A42MX36
Capacity						
System Gates	3,000	6,000	14,000	24,000	36,000	54,000
SRAM Bits	–	–	–	–	–	2,560
Logic Modules						
Sequential	–	–	348	624	954	1,230
Combinatorial	295	547	336	608	912	1,184
Decode	–	–	–	–	24	24
SRAM Modules (64x4 or 32x8)	–	–	–	–	–	10
Dedicated Flip-Flops	–	–	348	624	954	1,230
Maximum Flip-Flops	147	273	516	928	1,410	1,822
Clocks	1	1	2	2	2	6
Maximum User I/Os	57	69	104	140	176	202
Boundary Scan Test (BST)	No	No	No	No	Yes	Yes
Packages (by pin count)						
PLCC	68	84	84	–	–	–
PQFP	100	100	100, 160	208	160, 208	208, 240
VQFP	80	80	100	100	–	–
TQFP	–	–	176	176	176	–

Ordering Information



Plastic Device Resources

Device	User I/Os								
	PLCC 68-Pin	PLCC 84-Pin	PQFP 100-Pin	PQFP 160-Pin	PQFP 208-Pin	PQFP 240-Pin	VQFP 80-Pin	VQFP 100-Pin	TQFP 176-Pin
A40MX02	57	–	57	–	–	–	57	–	–
A40MX04	–	69	69	–	–	–	69	–	–
A42MX09	–	72	83	101	–	–	–	83	104
A42MX16	–	–	–	–	140	–	–	83	140
A42MX24	–	–	–	125	176	–	–	–	150
A42MX36	–	–	–	–	176	202	–	–	–

Package Definitions (Contact your Actel sales representative for product availability.)

PLCC = Plastic Leaded Chip Carrier, PQFP = Plastic Quad Flat Pack, TQFP = Thin Quad Flat Pack, VQFP = Very Thin Quad Flat Pack

Product Plan

	Speed Grade					Application				
	Std	–1	–2	–3	–F	C	I**	A*	M***	B***
A40MX02 Device										
44-Pin Plastic Leaded Chip Carrier (PLCC)	✔	✔	✔	✔	✔	✔	✔	–	✔	–
68-Pin Plastic Leaded Chip Carrier (PLCC)	✔	✔	✔	✔	✔	✔	✔	✔	✔	–
100-Pin Plastic Quad Flat Pack (PQFP)	✔	✔	✔	✔	✔	✔	✔	✔	✔	–
80-Pin Very Thin Plastic Quad Flat Pack (VQFP)	✔	✔	✔	✔	✔	✔	✔	✔	✔	–
A40MX04 Device										
44-Pin Plastic Leaded Chip Carrier (PLCC)	✔	✔	✔	✔	✔	✔	✔	–	✔	–
68-Pin Plastic Leaded Chip Carrier (PLCC)	✔	✔	✔	✔	✔	✔	✔	–	✔	–
84-Pin Plastic Leaded Chip Carrier (PLCC)	✔	✔	✔	✔	✔	✔	✔	✔	✔	–
100-Pin Plastic Quad Flat Pack (PQFP)	✔	✔	✔	✔	✔	✔	✔	✔	✔	–
80-Pin Very Thin Plastic Quad Flat Pack (VQFP)	✔	✔	✔	✔	✔	✔	✔	✔	✔	–
A42MX09 Device										
84-Pin Plastic Leaded Chip Carrier (PLCC)	✔	✔	✔	✔	✔	✔	✔	✔	✔	–
100-Pin Plastic Quad Flat Pack (PQFP)	✔	✔	✔	✔	✔	✔	✔	✔	✔	–
160-Pin Plastic Quad Flat Pack (PQFP)	✔	✔	✔	✔	✔	✔	✔	✔	✔	–
176-Pin Thin Plastic Quad Flat Pack (TQFP)	✔	✔	✔	✔	✔	✔	✔	✔	✔	–
100-Pin Very Thin Plastic Quad Flat Pack (VQFP)	✔	✔	✔	✔	✔	✔	✔	✔	✔	–
A42MX16 Device										
84-Pin Plastic Leaded Chip Carrier (PLCC)	✔	✔	✔	✔	✔	✔	✔	–	✔	–
100-Pin Plastic Quad Flat Pack (PQFP)	✔	✔	✔	✔	✔	✔	✔	–	✔	–
160-Pin Plastic Quad Flat Pack (PQFP)	✔	✔	✔	✔	✔	✔	✔	–	✔	–
208-Pin Plastic Quad Flat Pack (PQFP)	✔	✔	✔	✔	✔	✔	✔	✔	✔	–
176-Pin Thin Plastic Quad Flat Pack (TQFP)	✔	✔	✔	✔	✔	✔	✔	✔	✔	–
100-Pin Very Thin Plastic Quad Flat Pack (VQFP)	✔	✔	✔	✔	✔	✔	✔	✔	✔	–
A42MX24 Device										
84-Pin Plastic Leaded Chip Carrier (PLCC)	✔	✔	✔	✔	✔	✔	✔	–	✔	–
160-Pin Plastic Quad Flat Pack (PQFP)	✔	✔	✔	✔	✔	✔	✔	✔	✔	–
208-Pin Plastic Quad Flat Pack (PQFP)	✔	✔	✔	✔	✔	✔	✔	✔	✔	–
176-Pin Thin Plastic Quad Flat Pack (TQFP)	✔	✔	✔	✔	✔	✔	✔	✔	✔	–

Contact your Actel sales representative for product availability.

For more information on commercial-, industrial- and military-grade MX devices, refer to the 40MX and 42MX FPGA Families datasheet.

Applications:

C = Commercial
I = Industrial
A = Automotive
M = Military
B = MIL-STD-883 Class B

Availability:

✔ = Available
P = Planned
– = Not Planned

Speed Grade:

–1 = Approx. 15% faster than Standard
–2 = Approx. 25% faster than Standard
–3 = Approx. 35% faster than Standard
–F = Approx. 45% faster than Standard

* A is available in std only.
**I is available in std, –1, –2 and –3 only..
***M and B are offered only in -std and -1 only.

	Speed Grade					Application				
	Std	**–1**	**–2**	**–3**	**–F**	**C**	**I****	**A***	**M*****	**B*****
A42MX36 Device										
208-Pin Plastic Quad Flat Pack (PQFP)	✔	✔	✔	✔	✔	✔	✔	✔	✔	–
240-Pin Plastic Quad Flat Pack (PQFP)	✔	✔	✔	✔	✔	✔	✔	✔	✔	–
272-Pin Plastic Ball Grid Array (PBGA)	✔	✔	✔	✔	✔	✔	✔	–	✔	–
208-Pin Ceramic Quad Flat Pack (CQFP)	✔	✔	✔	–	–	✔	–	–	✔	✔
256-Pin Ceramic Quad Flat Pack (CQFP)	✔	✔	✔	–	–	✔	–	–	✔	✔

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* A is available in std only.
**I is available in std, –1, –2 and –3 only..
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Table of Contents

MX Automotive Family FPGAs

General Description

Actel's automotive-grade MX families provide a high-performance, single-chip solution for shortening the system design and development cycle, offering a cost-effective alternative to ASICs for in-cabin telematics and automobile interconnect applications. The 40MX and 42MX devices are excellent choices for integrating logic that is currently implemented in multiple PALs, CPLDs, and FPGAs.

The MX device architecture is based on Actel's patented antifuse technology implemented in a 0.45µ triple-metal CMOS process. With capacities ranging from 3,000 to 54,000 system gates, the synthesis-friendly automotive-grade MX devices are live on power-up, and require only one-fifth the standby power of comparable FPGAs. Actel's MX FPGAs provide up to 202 user I/Os and are available in a wide variety of packages and speed grades.

The automotive-grade A42MX24 and A42MX36 devices also include system-level features such as IEEE Standard 1149.1 (JTAG) Boundary Scan Testing, and fast wide-decode modules. The A42MX36 device offers dual-port SRAM for implementing fast FIFOs, LIFOs, and temporary data storage. The large number of storage elements can efficiently address applications requiring wide datapath manipulation and can perform transformation functions such as those required for telecommunications, networking, and DSP.

Power Requirements

Automotive-grade 40MX and 42MX devices operate in 5.0V systems.

40MX

V_{CC}	Input	Output
5.0V	5.0V	5.0V

42MX

$V_{CC}A$	V_{CCI}	Input	Output
5.0V	5.0V	5.0V	5.0V

MX Architectural Overview

The 40MX and 42MX devices are composed of fine-grained building blocks that enable fast, efficient logic designs. All devices within these families are composed of logic modules, I/O modules, routing resources, and clock networks, which are the building blocks for designing fast logic designs. In addition, the A42MX24 and A42MX36 devices contain wide decode modules, and the latter also contains embedded dual-port SRAM. The dual-port SRAM modules are optimized for high-speed datapath functions such as FIFOs, LIFOs, and scratchpad memory. "Product Profile" at the beginning of this document lists the specific logic resources contained within each device.

Logic Modules

The 40MX logic module is an eight-input, one-output logic circuit designed to implement a wide range of logic functions with efficient use of interconnect routing resources (Figure 1-1).

The logic module can implement the four basic logic functions (NAND, AND, OR, and NOR) in gates of two, three, or four inputs. Each function may have many versions with different combinations of active LOW inputs. The logic module can also implement a variety of D-latches, exclusivity functions, AND-ORs, and OR-ANDs. No dedicated hard-wired latches or flip-flops are required in the array; latches and flip-flops can be constructed from logic modules wherever needed in the application.

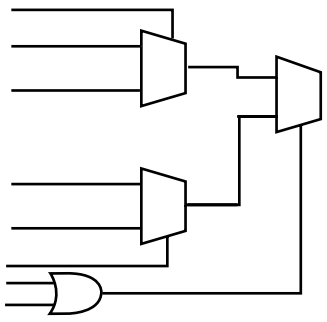


Figure 1-1 • **40MX Logic Module**

The 42MX devices contain three types of logic modules: combinatorial (C-modules), sequential (S-modules), and decode (D-modules).

The C-module, shown in Figure 1-2, implements the following function:

Y=!S1*!S0*D00+!S1*S0*D01+S1*!S0*D10+S1*S0*D11

where

S0=A0*B0

S1=A1+B1

The S-module, shown in Figure 1-3, is designed to implement high-speed sequential functions within a single logic module. The S-module implements the same combinatorial logic function as the C-module while adding a sequential element. The sequential element can be configured as either a D flip-flop or a transparent latch. To increase flexibility, the S-module register can be bypassed so that it implements purely combinatorial logic.

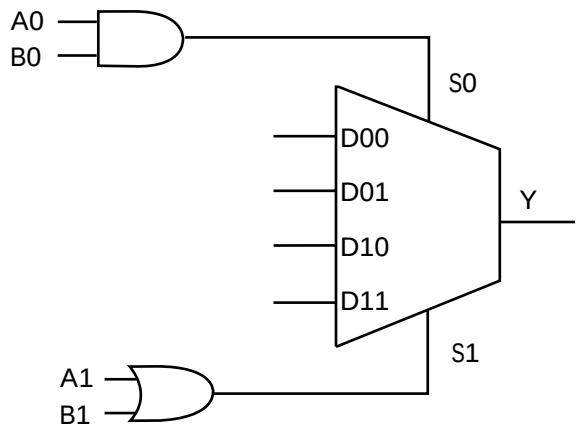
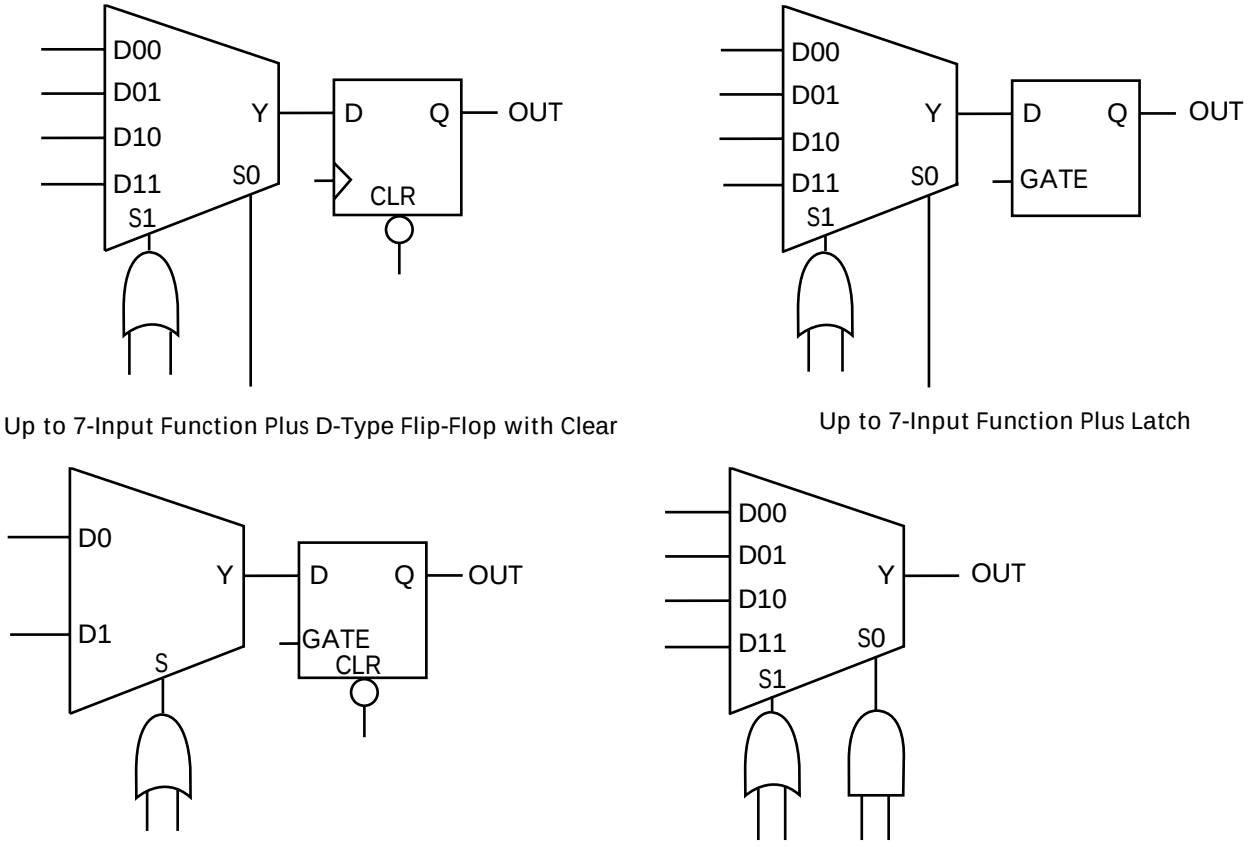


Figure 1-2 • **C-Module Implementation in 42MX Devices**



Up to 7-Input Function Plus D-Type Flip-Flop with Clear

Up to 7-Input Function Plus Latch

Up to 4-Input Function Plus Latch with Clear

Up to 7-Input Function Plus D-Type Flip-Flop with Clear

Figure 1-3 • **S-Module Implementation in 42MX Devices**

D-modules, available in A42MX24 and A42MX36 devices, contain wide-decode circuitry which provide a fast, wide-input AND function similar to that found in CPLD architectures (Figure 1-4). These modules are arranged around the periphery of the device. The D-module allows 42MX devices to perform wide-decode functions at speeds comparable to CPLDs and PALs. The output of the D-module has a programmable inverter for active HIGH or LOW assertion. The D-module output is hard-wired to an output pin, but it can also be fed back into the array to be incorporated into other logic.

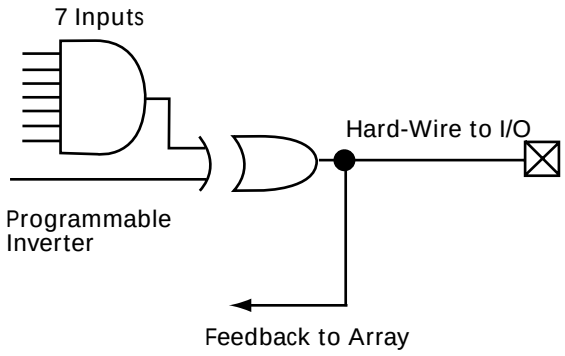


Figure 1-4 • **D-Module Implementation in 42MX Devices**

Dual-Port SRAM Modules

The A42MX36 device contains dual-port SRAM modules that have been optimized for synchronous or asynchronous applications. The SRAM modules are arranged in 256-bit blocks that can be configured as 32x8 or 64x4. SRAM modules can be cascaded together to form memory spaces of user-definable width and depth. A block diagram of the 42MX dual-port SRAM block is shown in Figure 1-5.

The 42MX SRAM modules are true dual-port structures containing independent read and write ports. Each SRAM module contains six bits of read and write addressing (RDAD[5:0] and WRAD[5:0], respectively) for 64x4-bit blocks. When configured in byte mode, the highest order address bits (RDAD5 and WRAD5) are not used. The read and write ports of the SRAM block contain independent clocks (RCLK and WCLK) with programmable polarities offering active HIGH or LOW implementation. The SRAM block contains eight data inputs (WD[7:0]), and eight outputs (RD[7:0]) which are connected to segmented vertical routing tracks.

The 42MX dual-port SRAM blocks provide an optimal solution for high-speed buffered applications requiring fast FIFO and LIFO queues. Actel's ACTgen Macro Builder provides the capability to quickly design memory functions, such as FIFOs, LIFOs, and RAM arrays. In addition, unused SRAM blocks can be used to implement registers for other logic within the design.

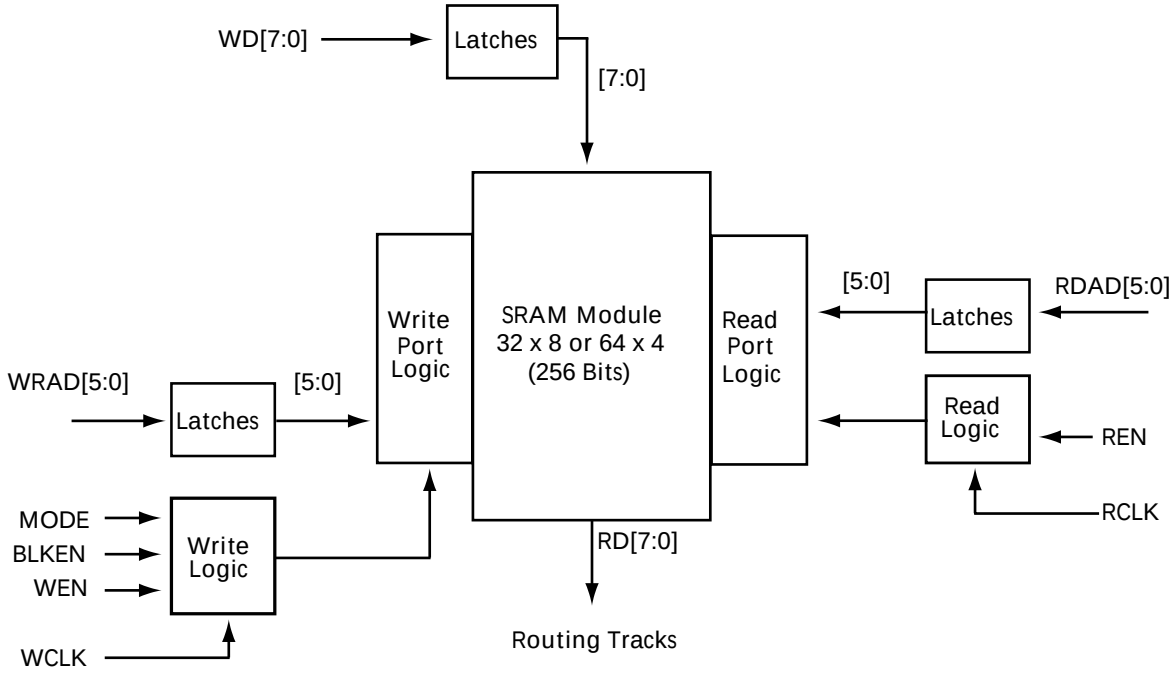


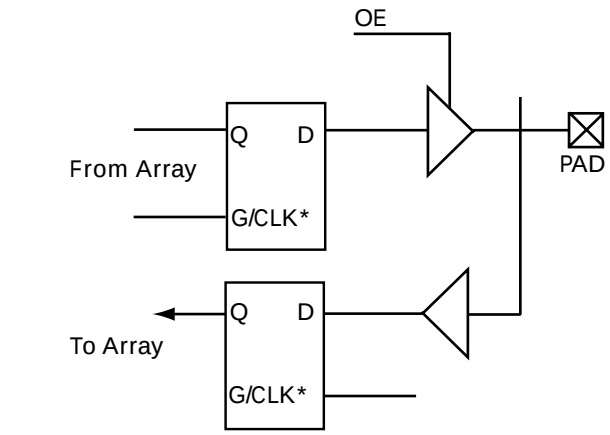
Figure 1-5 • **42MX Dual-Port SRAM Block**

MultiPlex I/O Modules

Automotive-grade 42MX devices offer MultiPlex I/Os, which support both 3.3V and 5.0V operations.

The MultiPlex I/O modules provide a flexible interface between the device pins and the logic array. Figure 1-6 is a block diagram of the 42MX I/O module. A variety of user functions, determined by a library macro selection, can be implemented in the module. (Refer to the *Macro Library Guide* for more information.) All 42MX I/O modules contain tri-state buffers, with input and output latches that can be configured for input, output, or bi-directional operation. Each output buffer has a dedicated output enable control. The I/O module can be used to latch input or output data, or both, providing a fast set-up time. In addition, the Actel Designer Series software tools can build a D-type flip-flop using a C-module to register input and output signals.

Actel's Designer Series development tools provide a design library of I/O macro functions that can implement all I/O configurations supported by the automotive-grade MX FPGAs.



Note: **Can be Configured as a Latch or D Flip-Flop (Using C-Module)*

Figure 1-6 • 42MX I/O Module

Routing Structure

The MX architecture uses vertical and horizontal routing tracks to interconnect the various logic and I/O modules. These routing tracks are metal interconnects that may be either of continuous length or broken into pieces called segments. Varying segment lengths allows the interconnect of over 90% of design tracks to occur with only two antifuse connections. Segments can be joined together at the ends using antifuses to increase their lengths up to the full length of the track. All interconnects can be accomplished with a maximum of four antifuses.

Horizontal Routing

Horizontal channels are located between the rows of modules and are composed of several routing tracks. The horizontal routing tracks within the channel are divided into one or more segments. The minimum horizontal segment length is the width of a module pair, and the maximum horizontal segment length is the full length of the channel. Any segment that spans more than one-third at the row length is considered a long horizontal segment. A typical channel is shown in Figure 1-7. Non-dedicated horizontal routing tracks are used to route signal nets; dedicated routing tracks are used for global clock networks and for power and ground tie-off tracks.

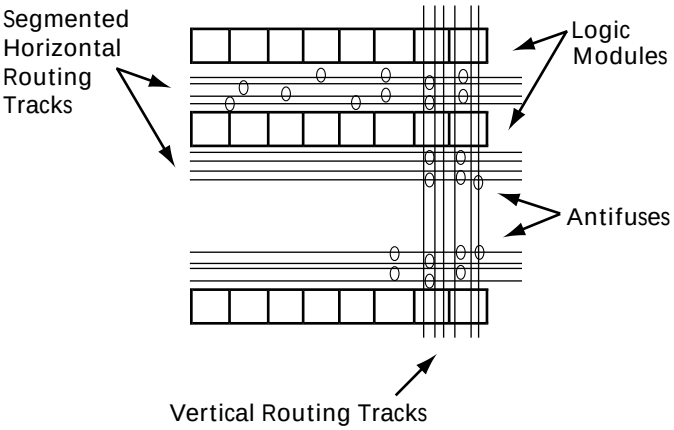


Figure 1-7 • Routing Structure

Vertical Routing

Another set of routing tracks run vertically through the module. There are three types of vertical tracks: input, output, and long, which are also divided into one or more segments. Each segment in an input track is dedicated to the input of a particular module; each segment in an output track is dedicated to the output of a particular module. Long segments are uncommitted and can be assigned during routing. Each output segment spans four channels (two above and two below), except near the top and bottom of the array, where edge effects occur. Long vertical tracks contain either one or two segments. An example of vertical routing tracks and segments is shown in Figure 1-7.

Antifuse Structures

An antifuse is a "normally open" structure as opposed to the normally connected fuse structure used in PROMs or PALs. The use of antifuses to implement a programmable logic device results in highly testable structures as well as efficient programming algorithms. The structure is highly-testable because there are no pre-existing connections; therefore, temporary connections can be made using pass transistors. These temporary connections can isolate individual antifuses to be programmed and individual circuit structures to be tested, which can be done before and after programming. For example, all metal tracks can be tested for continuity and shorts between adjacent tracks, and the functionality of all logic modules can be verified.

Clock Networks

The 40MX devices have one global clock distribution network (CLK). Two low-skew, high-fanout clock distribution networks are provided in each 42MX device. These networks are referred to as *CLK0* and *CLK1*. Each network has a clock module (CLKMOD) that selects the source of the clock signal and may be driven as follows:

- Externally from the CLKA pad
- Externally from the CLKB pad
- Internally from the CLKINTA input
- Internally from the CLKINTB input

The clock modules are located in the top row of I/O modules. Clock drivers and a dedicated horizontal clock track are located in each horizontal routing channel.

The user controls the clock module by selecting one of two clock macros from the macro library. The macro CLKBUF is used to connect one of the two external clock pins to a clock network, and the macro CLKINT is used to connect an internally-generated clock signal to a clock network. Since both clock networks are identical, it does not matter whether CLK0 or CLK1 is being used. The clock input pads can also be used as normal I/Os, bypassing the clock networks (Figure 1-8).

The A42MX36 device has four additional register control resources, called quadrant clock networks (Figure 1-9 on page 1-6). Each quadrant clock provides a local, high-fanout resource to the contiguous logic modules within its quadrant of the device. Quadrant clock signals can originate from specific I/O pins or from the internal array and can be used as a secondary register clock, register clear, or output enable.

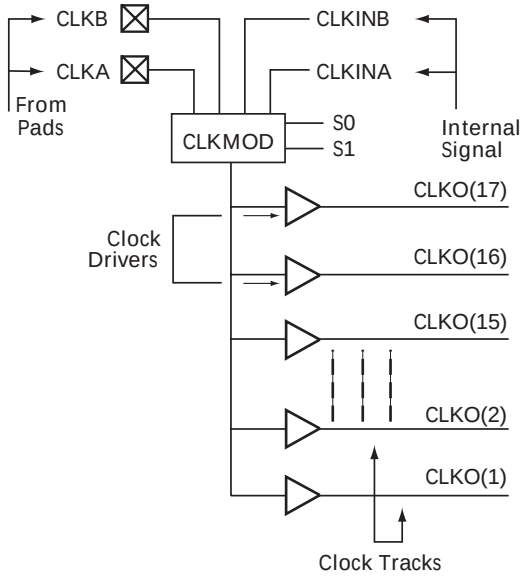


Figure 1-8 • 42MX Clock Networks

Test Circuitry

All MX automotive-grade devices contain probing circuitry which test and debug a design once it is programmed into a device. The test circuitry allows the designer to probe any internal node during device operation to aid in debugging a design.

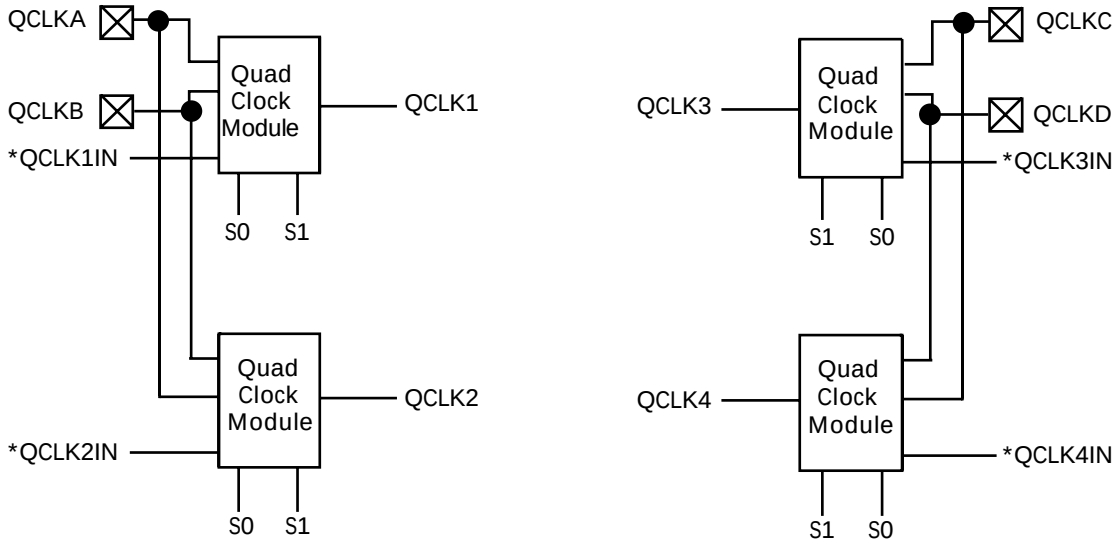
IEEE Standard 1149.1 Boundary Scan Testing (BST)

A42MX24 and A42MX36 devices contain IEEE Standard 1149.1 boundary scan test circuitry. IEEE Standard 1149.1 defines a four-pin Test Access Port (TAP) interface for testing integrated circuits in a system. The A42MX24 and A42MX36 devices provide the following BST pins: Test Data In (TDI), Test Data Out (TDO), Test Clock (TCK), and Test Mode Select (TMS). Devices are configured in a test "chain" where BST data can be transmitted serially between devices via TDO-to-TDI interconnections. The TMS and TCK signals are shared among all devices in the test chain so that all components operate in the same state.

The 42MX family implements a subset of the IEEE Standard 1149.1 BST instruction in addition to a private instruction. Refer to the IEEE Standard 1149.1 specification for detailed information regarding BST.

Boundary Scan Circuitry

The A42MX24 and A42MX36 boundary-scan circuitry consists of a Test Access Port (TAP) controller, test instruction register, a bypass register, and a boundary scan register. Figure 1-10 on page 1-6 shows a block diagram of the 42MX boundary scan circuitry.



*QCLK1IN, QCLK2IN, QCLK3IN, and QCLK4IN are internally-generated signals.

Figure 1-9 • **A42MX36 Quadrant Clock Network**

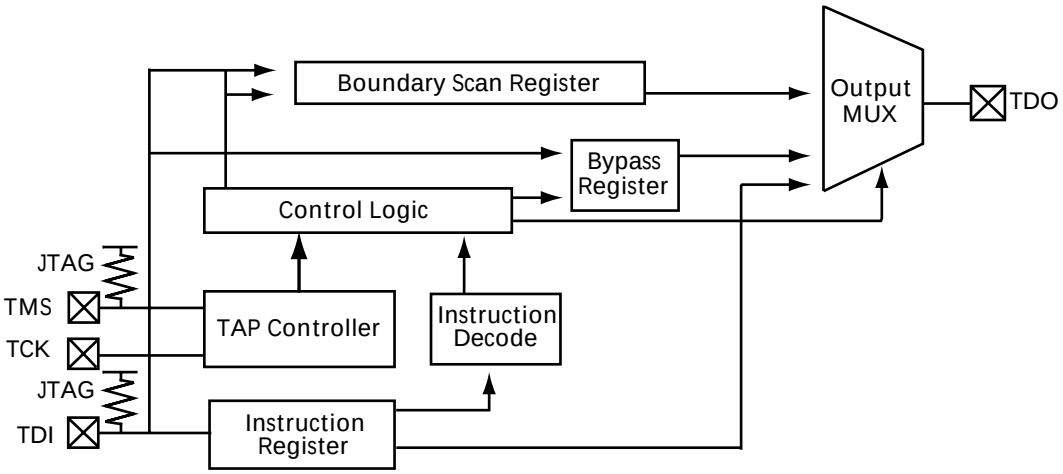


Figure 1-10 • **IEEE 1149.1 Boundary Scan Circuitry in A42MX24 and A42MX36**

When a device is operating in BST mode, four I/O pins are used for the TDI, TDO, TMS, and TCK signals. An active reset (TRST) pin is not supported; however, the A42MX24 and A42MX36 devices contain power-on circuitry that resets the boundary scan circuitry upon power-up. Table 1-1 summarizes the functions of the IEEE 1149.1 BST signals.

***Table 1-1* • IEEE 1149.1 BST Signals**

Signal	Name	Function
TDI	Test Data In	Serial data input for BST instructions and data. Data is shifted in on the rising edge of TCK.
TDO	Test Data Out	Serial data output for BST instructions and test data.
TMS	Test Mode Select	Serial data input for BST mode. Data is shifted in on the rising edge of TCK.
TCK	Test Clock	Clock signal to shift the BST data into the device.

JTAG

A42MX24 and A42MX36 automotive-grade MX devices offer superior diagnostic and testing capabilities by providing JTAG and probing capabilities. These functions are controlled through the special JTAG pins in conjunction with the program fuse.

JTAG fuse programmed:

- TCK must be terminated—logical high or low doesn't matter (to avoid floating input)
- TDI, TMS may float or at logical high (internal pull-up is present)
- TDO may float or connect to TDI of another device (it's an output)
- JTAG fuse not programmed:
- TCK, TDI, TDO, TMS are user I/O. If not used, they will be configured as tri-stated output.

BST Instructions

Boundary scan testing within the A42MX24 and A42MX36 devices is controlled by a Test Access Port (TAP) state machine. The TAP controller drives the three-bit instruction register, a bypass register, and the boundary scan data registers within the device. The TAP controller uses the TMS signal to control the testing of the device. The BST mode is determined by the bitstream entered on the TMS pin. Table 1-2 describes the test instructions supported by the A42MX24 and A42MX36 devices.

***Table 1-2* • BST Instructions**

Test Mode	Code	Description
EXTEST	000	Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
SAMPLE/ PRELOAD	001	Allows a snapshot of the signals at the device pins to be captured and examined during device operation.
HIGH Z	101	Refer to the IEEE Standard 1149.1 specification.
CLAMP	110	Refer to the IEEE Standard 1149.1 specification.
BYPASS	111	Enables the bypass register between the TDI and TDO pins. The test data passes through the selected device to adjacent devices in the test chain.

Reset

The TMS pin is equipped with an internal pull-up resistor. This allows the TAP controller to remain in or return to the Test-Logic-Reset state when there is no input or when a logical 1 is on the TMS pin. To reset the controller, TMS must be HIGH for at least five TCK cycles.

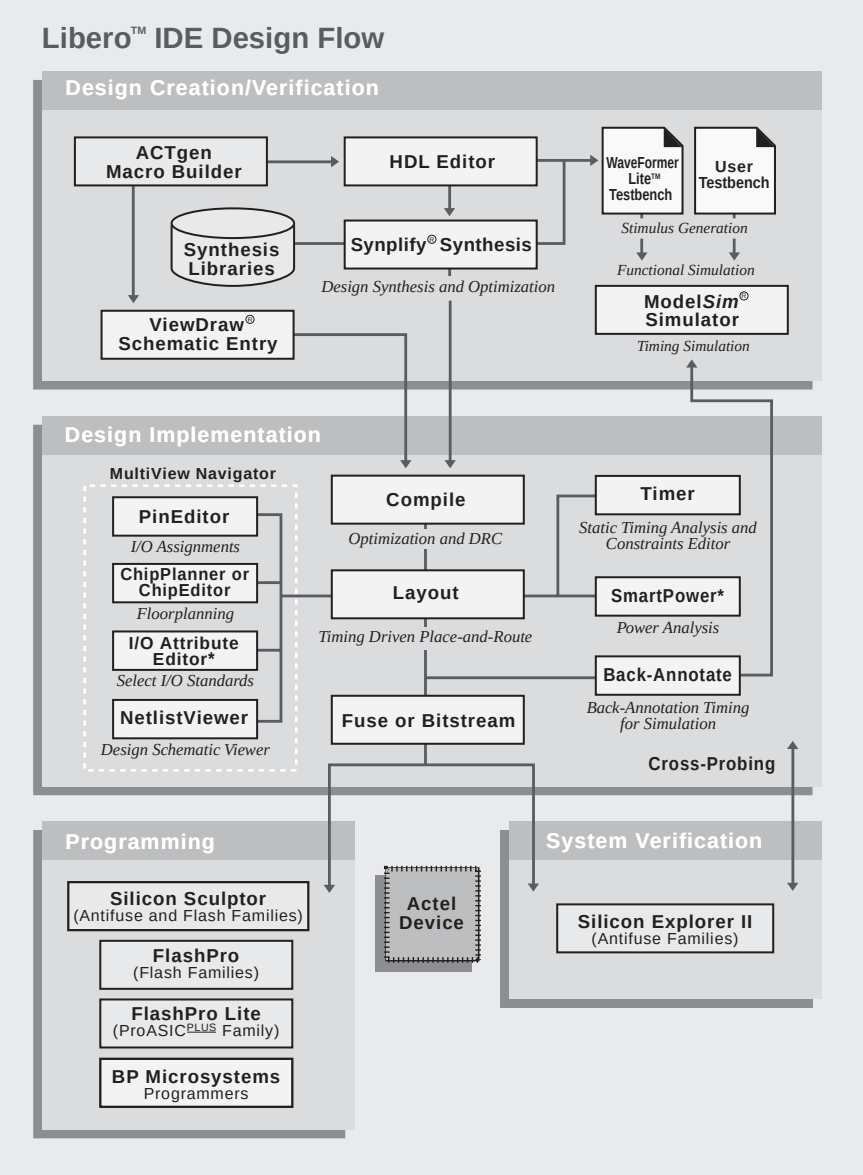
Development Tool Support

The automotive-grade MX family of FPGAs is fully supported by both Actel's Libero™ Integrated Design Environment and Designer FPGA Development software. Actel Libero IDE is a design management environment that streamlines the design flow. Libero IDE provides an integrated design manager that seamlessly integrates design tools while guiding the user through the design flow, managing all design and log files, and passing necessary design data among tools. Additionally, Libero IDE allows users to integrate both schematic and HDL synthesis into a single flow and verify the entire design in a single environment (Figure 1-11 on page 1-8). Libero IDE includes Synplify® for Actel from Synplicity®, ViewDraw for Actel from Mentor Graphics, Model*Sim*™ HDL Simulator from Model Technology™, WaveFormer Lite™ from SynaptiCAD™, and Designer software from Actel.

Actel's Designer software provides a comprehensive suite of backend development tools for FPGA development. The Designer software includes timing-driven place-and-route, and a world-class integrated static timing analyzer and constraints editor. With the Designer software, a user can lock his/her design pins before layout while minimally impacting the results of place-and-route. Additionally, the back-annotation flow is compatible

with all the major simulators and the simulation results can be cross-probed with Silicon Explorer II, Actel's integrated verification and logic analysis tool. Another tool included in the Designer software is the ACTgen macro builder, which easily creates popular and commonly used logic functions for implementation into your schematic or HDL design.

Actel's Designer software is compatible with the most popular FPGA design entry and verification tools from companies such as Mentor Graphics, Synplicity, Synopsys, and Cadence Design Systems. The Designer software is available for both the Windows and Unix operating systems.



Note: **Only available in Axcelerator and ProASIC^{PLUS} Devices.*

Figure 1-11 • **Design Flow**

5.0V Operating Conditions

Absolute Maximum Ratings*

Free Air Temperature Range

Symbol	Parameter	Limits	Units
$V_{CC}/V_{CCA}/V_{CCI}$	DC Supply Voltage	–0.5 to +6.5	V
V_I	Input Voltage	–0.5 to V_{CC} +0.5	V
V_O	Output Voltage	–0.5 to V_{CC} +0.5	V
T_{STG}	Storage Temperature	–65 to +150	°C

Note: **Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the Recommended Operating Conditions.*

Recommended Operating Conditions

Parameter	Automotive	Units
Temperature Range*	-40 to +125	°C
V_{CCI}	4.75 to 5.25	V
V_{CCA}	4.75 to 5.25	V
V_{CC}	4.75 to 5.25	V

Note: **Ambient temperature (T_A)*

Electrical Specifications

Symbol	Parameter	Automotive		Units
		Min.	Max.	
V_{OH}	(I_{OH} = –4 mA)	3.1		V
V_{OL}	(I_{OL} = 4 mA)		0.4	V
V_{IL}			0.6	V
V_{IH}		2.1		V
I_{IL}		–20	20	µA
I_{IH}		–20	20	µA
Input Transition Time t_R, t_F[1]			250	ns
C_{IO} I/O Capacitance[1, 2]			10	pF
Standby Current, I_{CC}[3]			35	mA
$I_{CC(D)}$ Dynamic V_{CCI} Supply Current		See "Power Dissipation" on page 1-10.		

1. Not tested, for information only.
2. Includes worst-case 84-pin PLCC package capacitance. V_{OUT} = 0 V, f = 1 MHz.
3. All outputs unloaded. All inputs = V_{CC} or GND.

Package Thermal Characteristics

The device junction-to-case thermal characteristic is θ_{jc}, and the junction-to-ambient air characteristic is θ_{ja}. The thermal characteristics for θ_{ja} are shown with two different air flow rates.

Maximum junction temperature is 150°C.

A sample calculation of the absolute maximum power dissipation allowed for a PQFP 160-pin package at commercial temperature is as follows:

$$\frac{\text{Max. junction temp. (°C)} - \text{Max. commercial temp.}}{\theta_{ja}\ (°C/W)} = \frac{150°C - 125°C}{32°C/W} = 0.78W$$

			θ_{ja}	
Plastic Packages	**Pin Count**	θ_{jc}	**Still Air**	**300 ft/min**
Plastic Quad Flat Pack	100	12	34°C/W	31°C/W
Plastic Quad Flat Pack	160	10	32°C/W	24°C/W
Plastic Quad Flat Pack	208	8	30°C/W	23°C/W
Plastic Quad Flat Pack	240	3.5	19°C/W	16°C/W
Plastic Leaded Chip Carrier	68	13	36°C/W	25°C/W
Plastic Leaded Chip Carrier	84	12	32°C/W	22°C/W
Thin Plastic Quad Flat Pack	176	11	28°C/W	21°C/W
Very Thin Plastic Quad Flat Pack	80	12	39°C/W	33°C/W
Very Thin Plastic Quad Flat Pack	100	10	38°C/W	32°C/W

Power Dissipation

General Power Equation

$$P = [I_{CC}standby + I_{CC}active] * V_{CCI} + I_{OL} * V_{OL} * N + I_{OH} * (V_{CCI} - V_{OH}) * M$$

where:

$I_{CC}standby$ is the current flowing when no inputs or outputs are changing.

$I_{CC}active$ is the current flowing due to CMOS switching.

I_{OL}, I_{OH} are TTL sink/source currents.

V_{OL}, V_{OH} are TTL level output voltages.

N equals the number of outputs driving TTL loads to V_{OL}.

M equals the number of outputs driving TTL loads to V_{OH}.

Accurate values for N and M are difficult to determine because they depend on the family type, on design details, and on the system I/O. The power can be divided into two components: static and active.

Static Power Component

Actel FPGAs have small static power components that result in power dissipation lower than PALs or CPLDs. By integrating multiple PALs/CPLDs into one FPGA, an even greater reduction in board-level power dissipation can be achieved.

The power due to standby current is typically a small component of the overall power.

The static power dissipation by TTL loads depends on the number of outputs driving HIGH or LOW, and on the DC load current. Again, this number is typically small. For instance, a 32-bit bus sinking 4 mA at 0.33V will generate 42 mW with all outputs driving LOW, and 140 mW with all outputs driving HIGH. The actual dissipation will average somewhere in between, as I/Os switch states with time.

Active Power Component

Power dissipation in CMOS devices is usually dominated by the active (dynamic) power dissipation. This component is frequency-dependent and a function of the logic and the external I/O. Active power dissipation results from charging internal chip capacitances of the interconnect, unprogrammed antifuses, module inputs, and module outputs, plus external capacitance due to PC board traces and load device inputs. An additional component of the active power dissipation is the totem pole current in the CMOS transistor pairs. The net effect can be associated with an equivalent capacitance that can be combined with frequency and voltage to represent active power dissipation.

Equivalent Capacitance

The power dissipated by a CMOS circuit can be expressed by the equation:

$$\text{Power } (\mu W) = C_{EQ} * V_{CCA}^2 * F$$

EQ 1-1

where:

C_{EQ} = Equivalent capacitance expressed in picofarads (pF)

V_{CCA} = Power supply in volts (V)

F = Switching frequency in megahertz (MHz)

Equivalent capacitance is calculated by measuring I_{CC}active at a specified frequency and voltage for each circuit component of interest. Measurements have been made over a range of frequencies at a fixed value of V_{CC}. Equivalent capacitance is frequency-independent, so the results can be used over a wide range of operating conditions. Equivalent capacitance values are shown below.

C_{EQ} Values for Actel MX FPGAs

Modules (C_{EQM})	3.5
Input Buffers (C_{EQI})	6.9
Output Buffers (C_{EQO})	18.2
Routed Array Clock Buffer Loads (C_{EQCR})	1.4

To calculate the active power dissipated from the complete design, the switching frequency of each part of the logic must be known. The equation below shows a piece-wise linear summation over all components.

$$\text{Power} = V_{CCA}^2 * [(m \times C_{EQM} * f_m)_{Modules} + (n * C_{EQI} * f_n)_{Inputs} + (p * (C_{EQO} + C_L) * f_p)_{outputs} + 0.5 * (q_1 * C_{EQCR} * f_{q1})_{routed\_Clk1} + (r_1 * f_{q1})_{routed\_Clk1} + 0.5 * (q_2 * C_{EQCR} * f_{q2})_{routed\_Clk2} + (r_2 * f_{q2})_{routed\_Clk2}$$

EQ 1-2

where:

m = Number of logic modules switching at frequency f_m

n = Number of input buffers switching at frequency f_n

p = Number of output buffers switching at frequency f_p

q_1 = Number of clock loads on the first routed array clock

q_2 = Number of clock loads on the second routed array clock

r_1 = Fixed capacitance due to first routed array clock

r_2 = Fixed capacitance due to second routed array clock

C_{EQM} = Equivalent capacitance of logic modules in pF

C_{EQI} = Equivalent capacitance of input buffers in pF

C_{EQO} = Equivalent capacitance of output buffers in pF

C_{EQCR} = Equivalent capacitance of routed array clock in pF

C_L = Output load capacitance in p

f_m = Average logic module switching rate in MHz

f_n = Average input buffer switching rate in MHz

f_p = Average output buffer switching rate in MHz

f_{q1} = Average first routed array clock rate in MHz

f_{q2} = Average second routed array clock rate in MHz

Fixed Capacitance Values for MX FPGAs (pF)

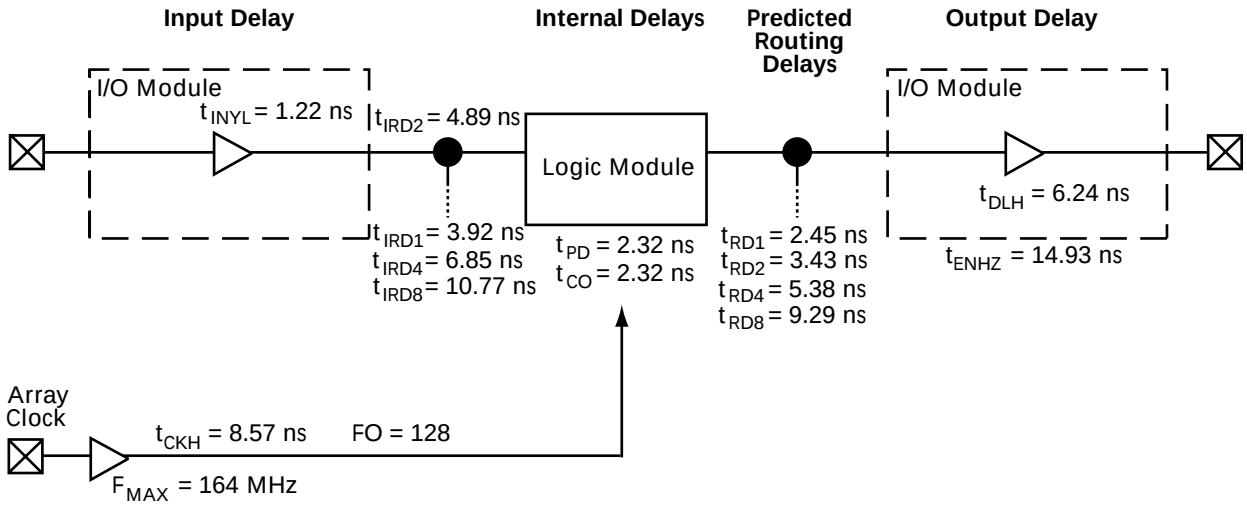
Device Type	r1 routed_Clk1	r2 routed_Clk2
A40MX02	41.4	N/A
A40MX04	68.6	N/A
A42MX09	118	118
A42MX16	165	165
A42MX24	185	185
A42MX36	220	220

Determining Average Switching Frequency

To determine the switching frequency for a design, the data input values to the circuit must be clearly understood. The following guidelines represent worst-case scenarios; these can be used to generally predict the upper limits of power dissipation.

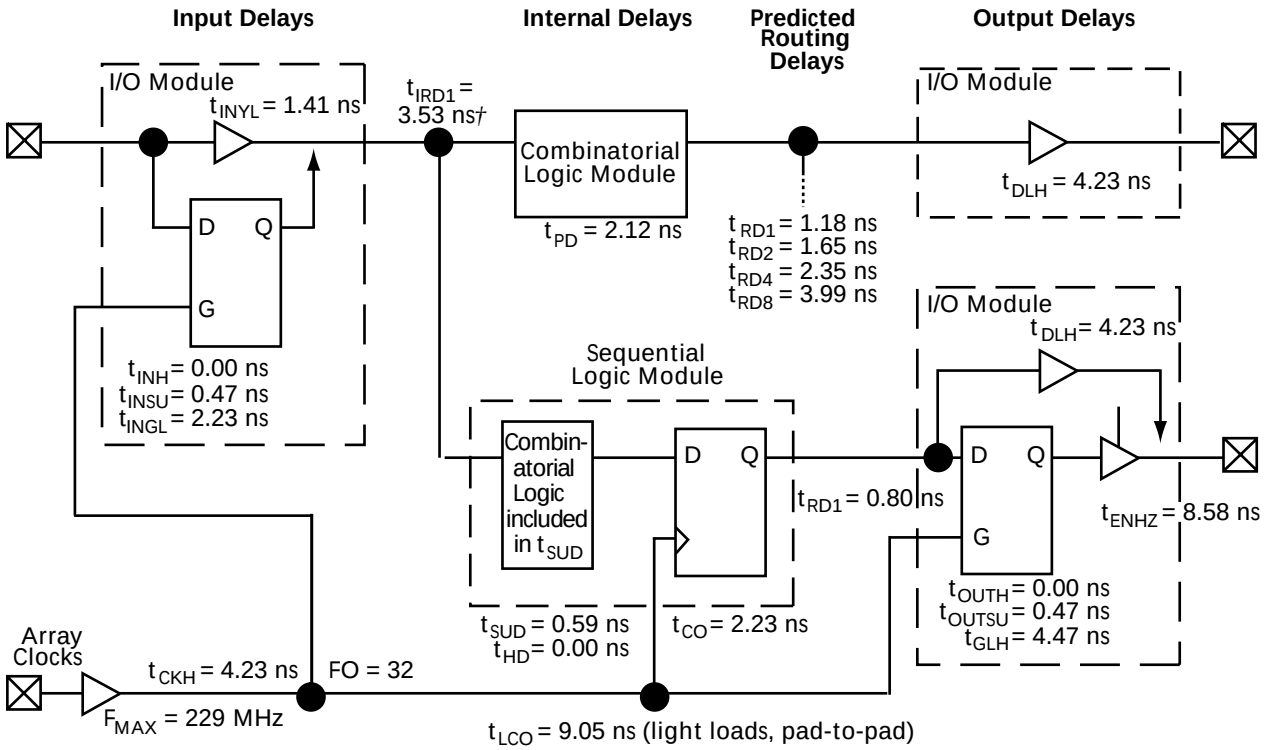
Logic Modules (m)	=	80% of Combinatorial Modules
Inputs Switching (n)	=	# of Inputs/4
Outputs Switching (p)	=	# of Outputs/4
First Routed Array Clock Loads (q_1)	=	40% of Sequential Modules
Second Routed Array Clock Loads (q_2)	=	40% of Sequential Modules
Load Capacitance (C_L)	=	35 pF
Average Logic Module Switching Rate (f_m)	=	F/10
Average Input Switching Rate (f_n)	=	F/5
Average Output Switching Rate (f_p)	=	F/10
Average First Routed Array Clock Rate (f_{q1})	=	F
Average Second Routed Array Clock Rate (f_{q2})	=	F/2

Timing Information



* Values are shown for 40MX at worst-case 5.0V automotive conditions.

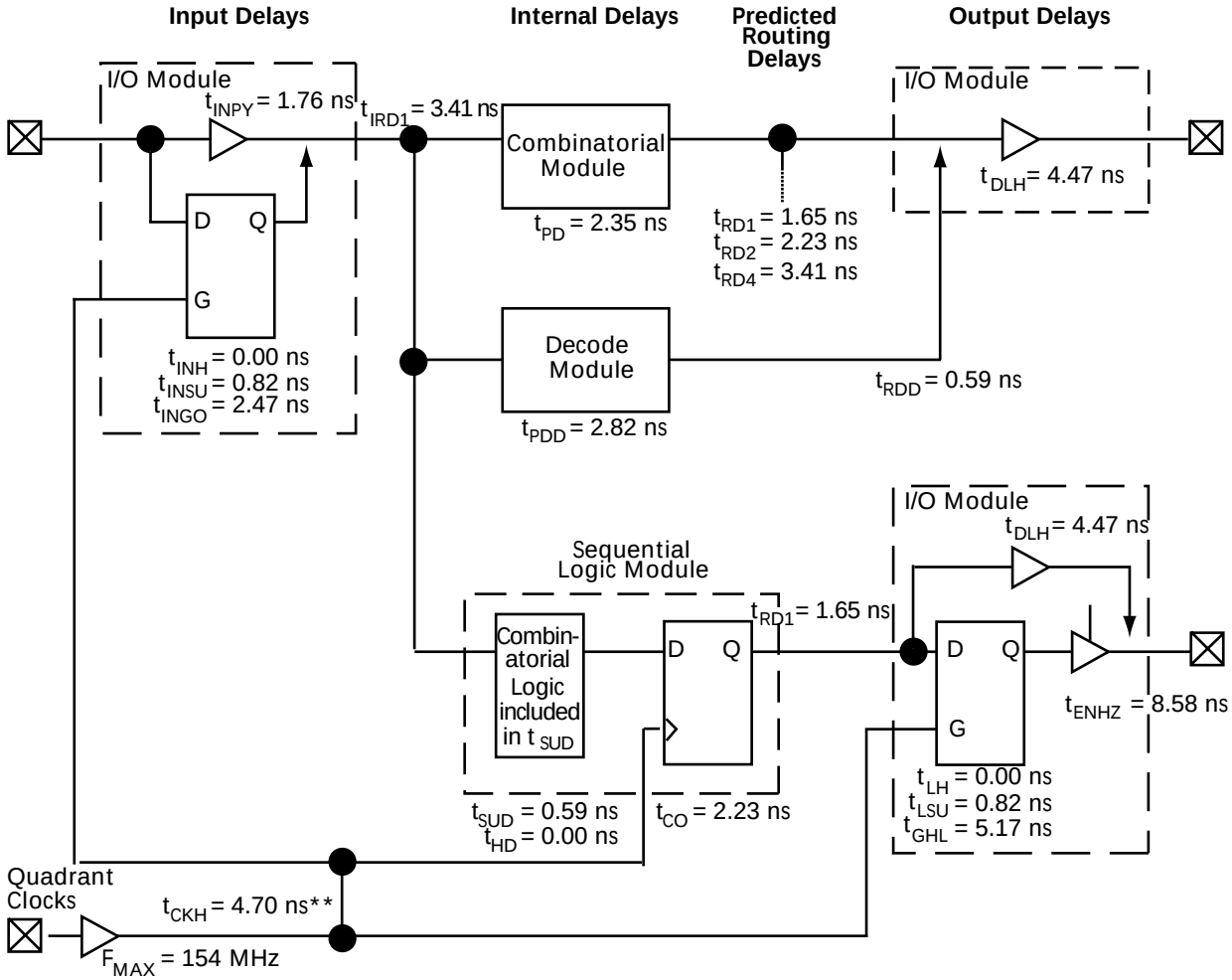
Figure 1-12 • **40MX Timing Model***



*Values are shown for A42MX09 at worst-case 5.0V automotive conditions

† Input module predicted routing delay

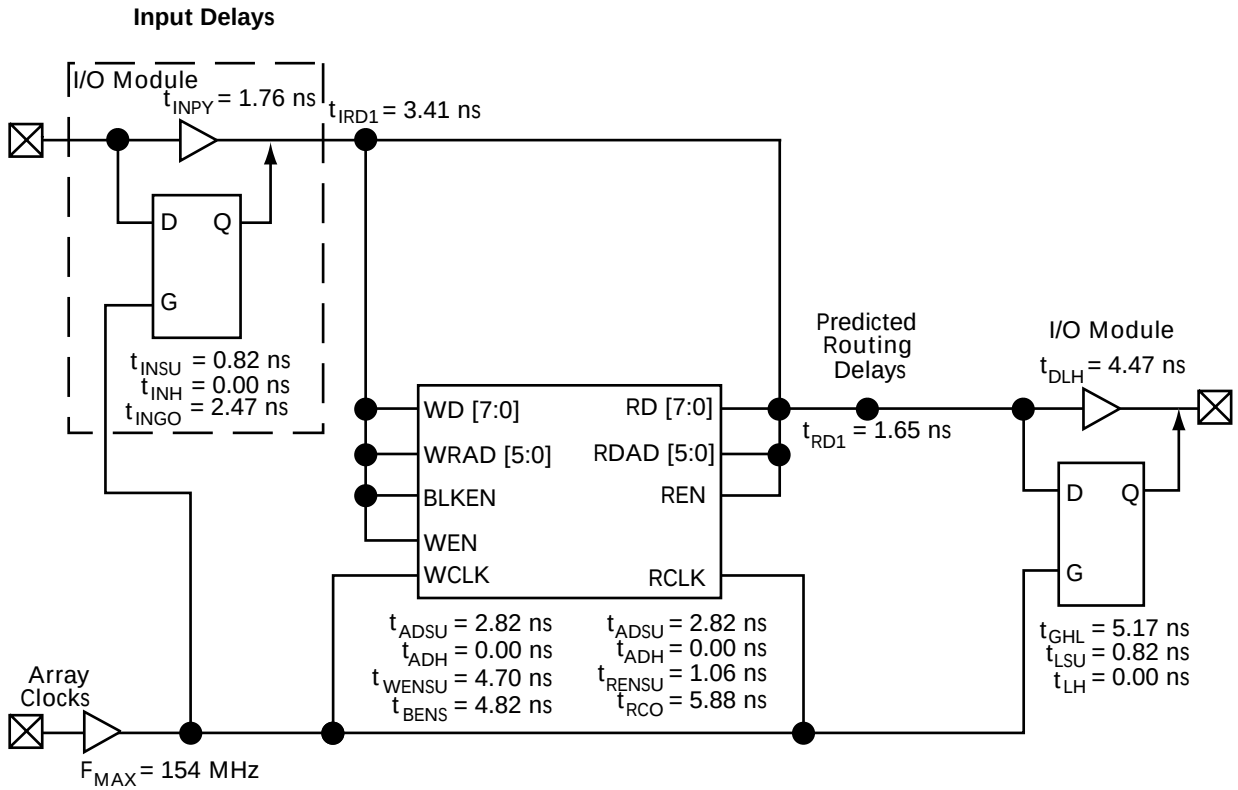
Figure 1-13 • **42MX Timing Model***



* Preliminary values are shown for A42MX36 at worst-case 5.0V automotive conditions

** Load-dependent

Figure 1-14 • **A42MX36 Timing Model (Logic Functions using Quadrant Clocks)***



*Values are shown for A42MX36 at worst-case 5.0V automotive conditions.

Figure 1-15 • **A42MX36 Timing Model (SRAM Functions)***

Parameter Measurement

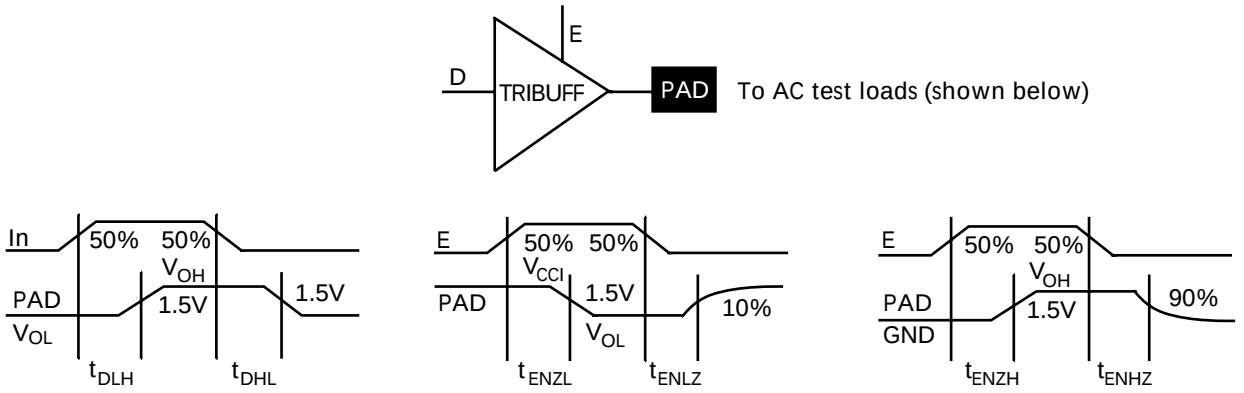


***Figure 1-16* • Output Buffer Delays**

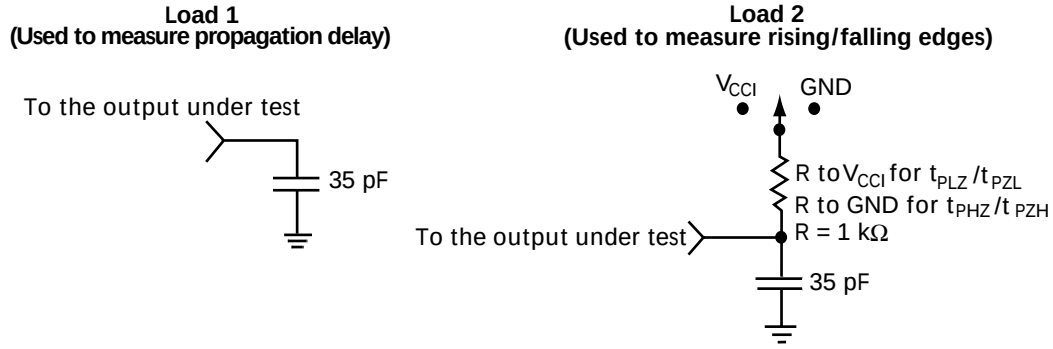


***Figure 1-17* • AC Test Loads**

Sequential Timing Characteristics

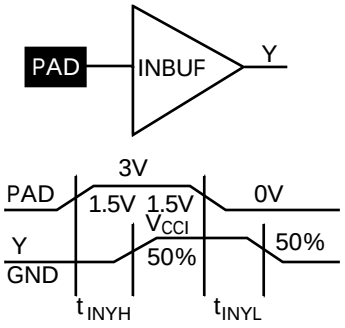


Figure 1-18 • **Input Buffer Delays**

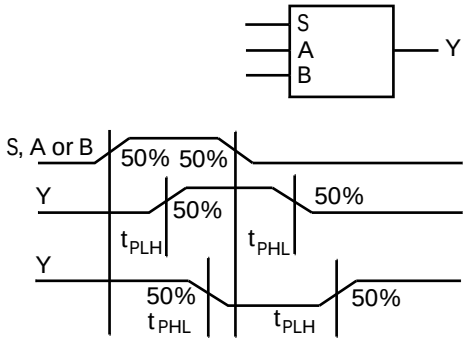
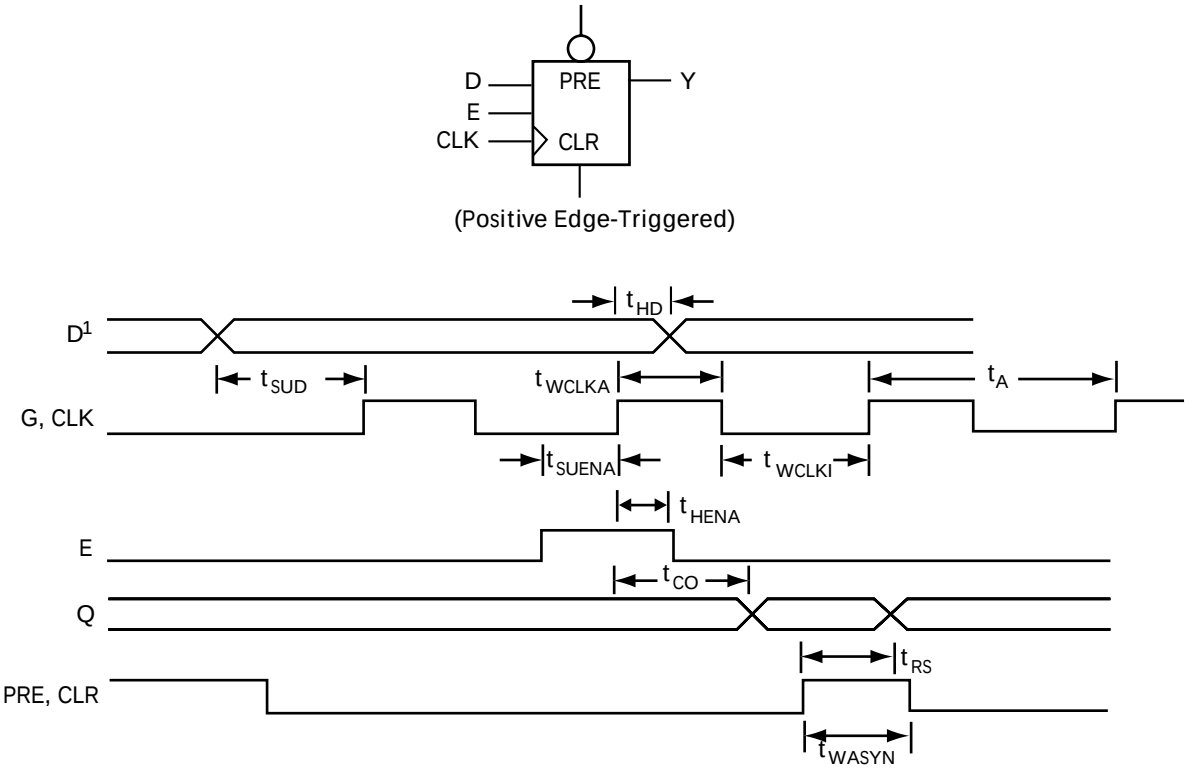


Figure 1-19 • **Module Delays**



D represents all data functions involving A. B. and S for multiplexed flip-flops.

Figure 1-20 • **Flip-Flops and Latches**

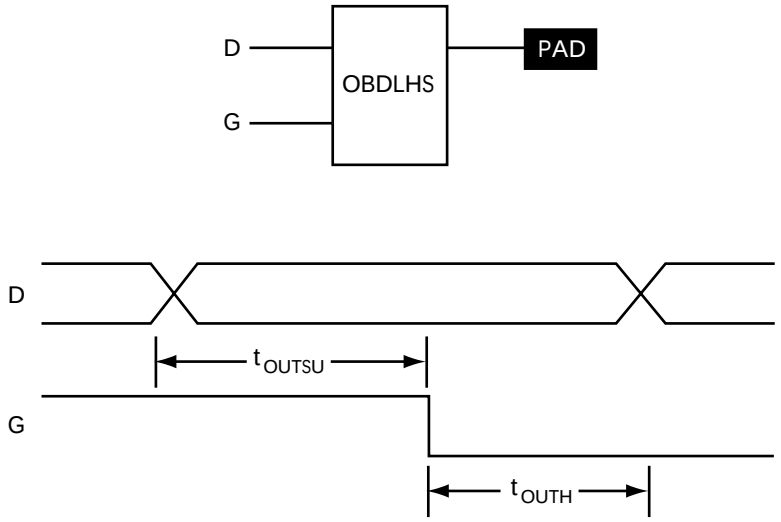


Figure 1-22 • **Output Buffer Latches**

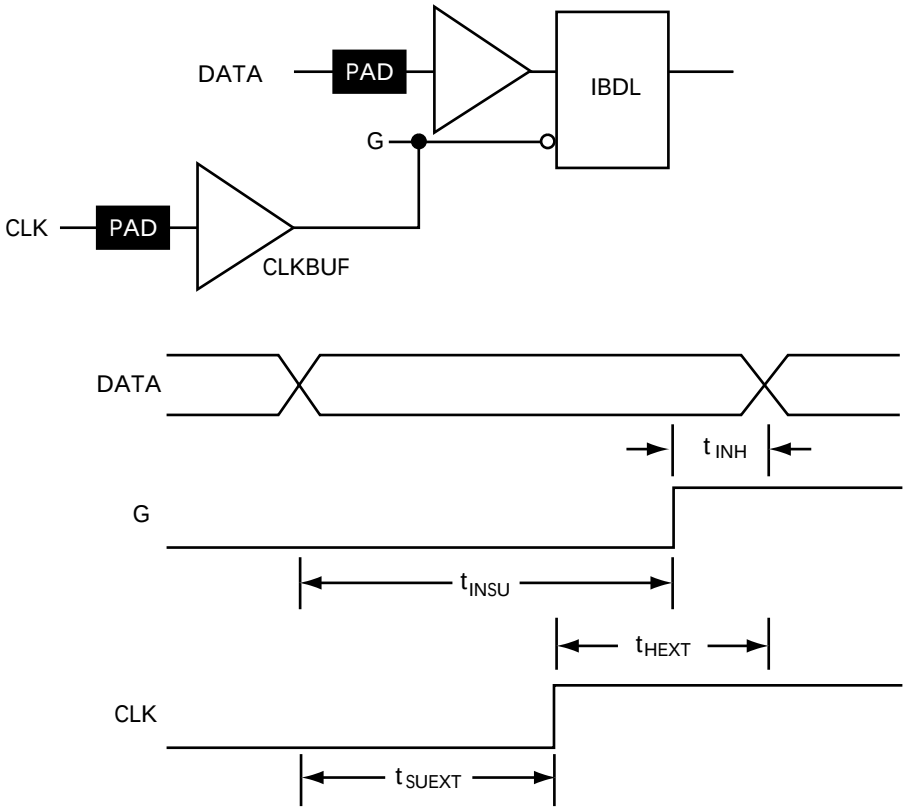


Figure 1-21 • **Input Buffer Latches**

Decode Module Timing

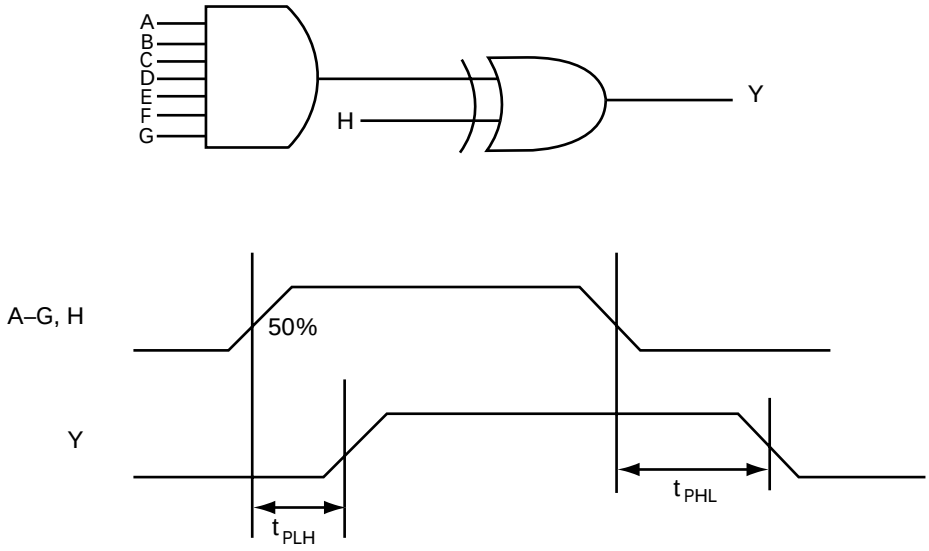


Figure 1-23 • **Decode Module Timing**

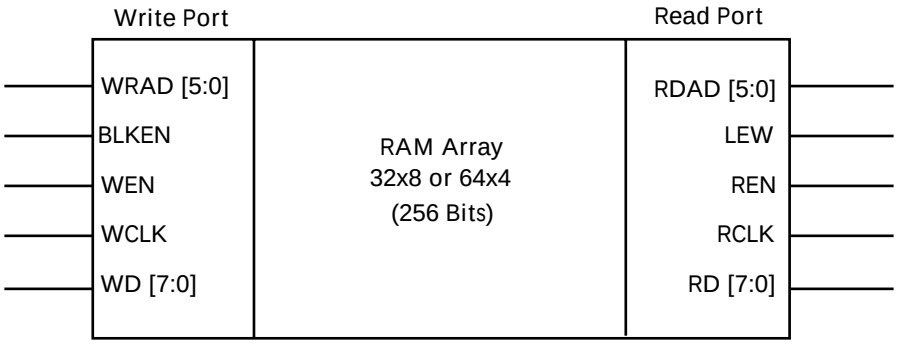
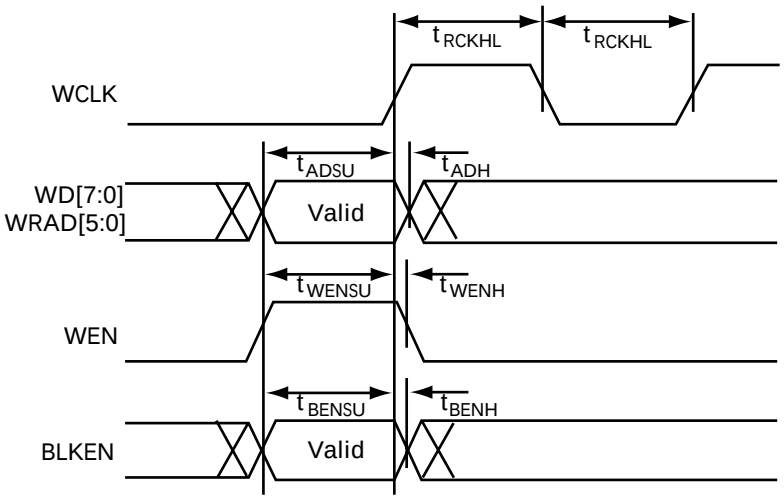


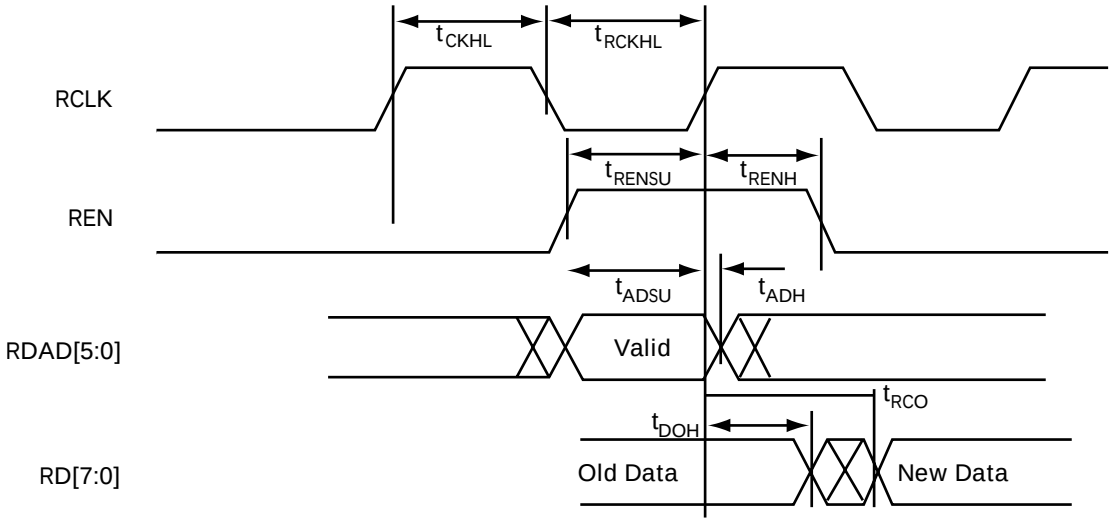
Figure 1-24 • **SRAM Timing Characteristics**

Dual-Port SRAM Timing Waveforms



Note: *Identical timing for falling edge clock.*

Figure 1-25 • 42MX SRAM Write Operation



Note: *Identical timing for falling edge clock.*

Figure 1-26 • 42MX SRAM Synchronous Read Operation

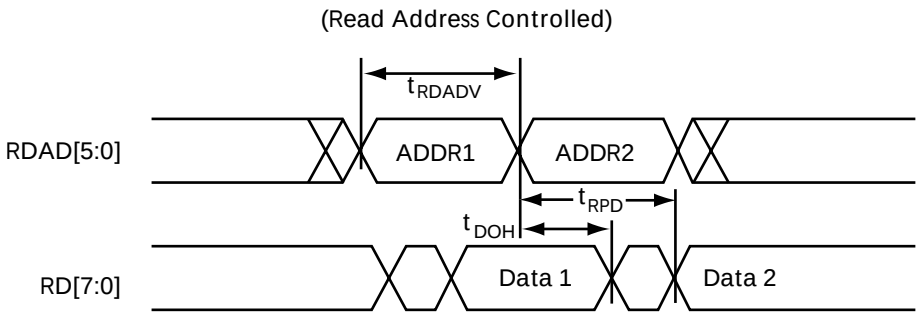


Figure 1-27 • 42MX SRAM Asynchronous Read Operation—Type 1

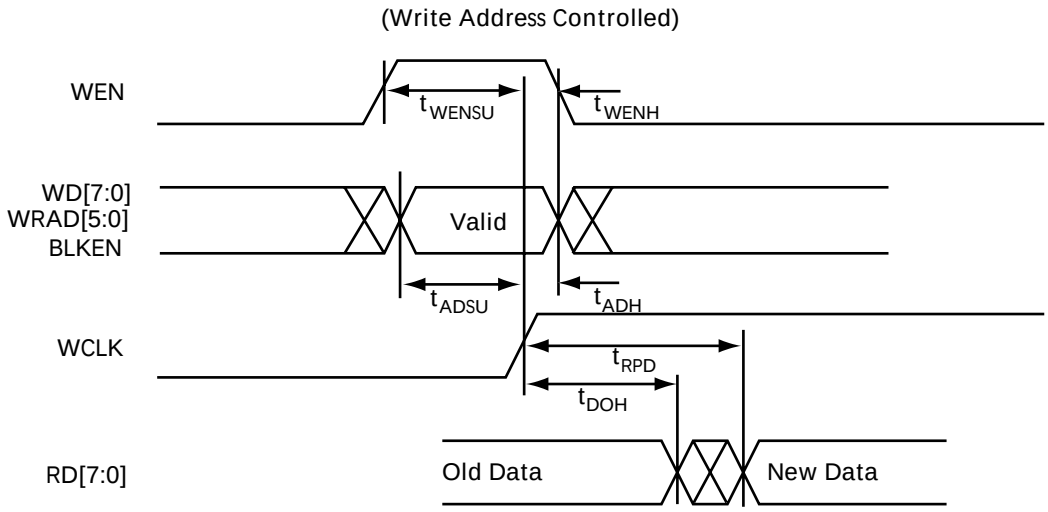


Figure 1-28 • 42MX SRAM Asynchronous Read Operation—Type 2

Predictable Performance: Tight Delay Distributions

Propagation delay between logic modules depends on the resistive and capacitive loading of the routing tracks, the interconnect elements, and the module inputs being driven. Propagation delay increases as the length of routing tracks, the number of interconnect elements, or the number of inputs increases.

From a design perspective, the propagation delay can be statistically correlated or modeled by the fanout (number of loads) driven by a module. Higher fanout usually requires some paths to have longer routing tracks.

The MX FPGAs deliver a tight fanout delay distribution, which is achieved in two ways: by decreasing the delay of the interconnect elements and by decreasing the number of interconnect elements per path.

Actel's patented antifuse offers a very low resistive/capacitive interconnect. The antifuses, fabricated in 0.45 µ lithography, offer nominal levels of 100 Ω resistance and 7.0 femtofarad (fF) capacitance per antifuse.

MX fanout distribution is also tight due to the low number of antifuses required for each interconnect path. The proprietary architecture limits the number of antifuses per path to a maximum of four, with 90 percent of interconnects using only two antifuses.

Timing Characteristics

Device timing characteristics fall into three categories: family-dependent, device-dependent, and design-dependent. The input and output buffer characteristics are common to all MX devices. Internal routing delays are device-dependent. Design dependency means actual delays are not determined until after place-and-route of the user's design is complete. Delay values may then be determined by using the Designer Series utility or by performing simulation with post-layout delays.

Critical Nets and Typical Nets

Propagation delays in this data sheet apply to typical nets. The abundant routing resources in the MX architecture allows for deterministic timing using Actel's Designer Series development tools, which include TDPR, a timing-driven place-and-route tool. Using Timer, the designer can specify timing-critical nets and system clock frequency. Using these timing specifications, the place-and-route software optimizes the layout of the design to meet the user's specifications.

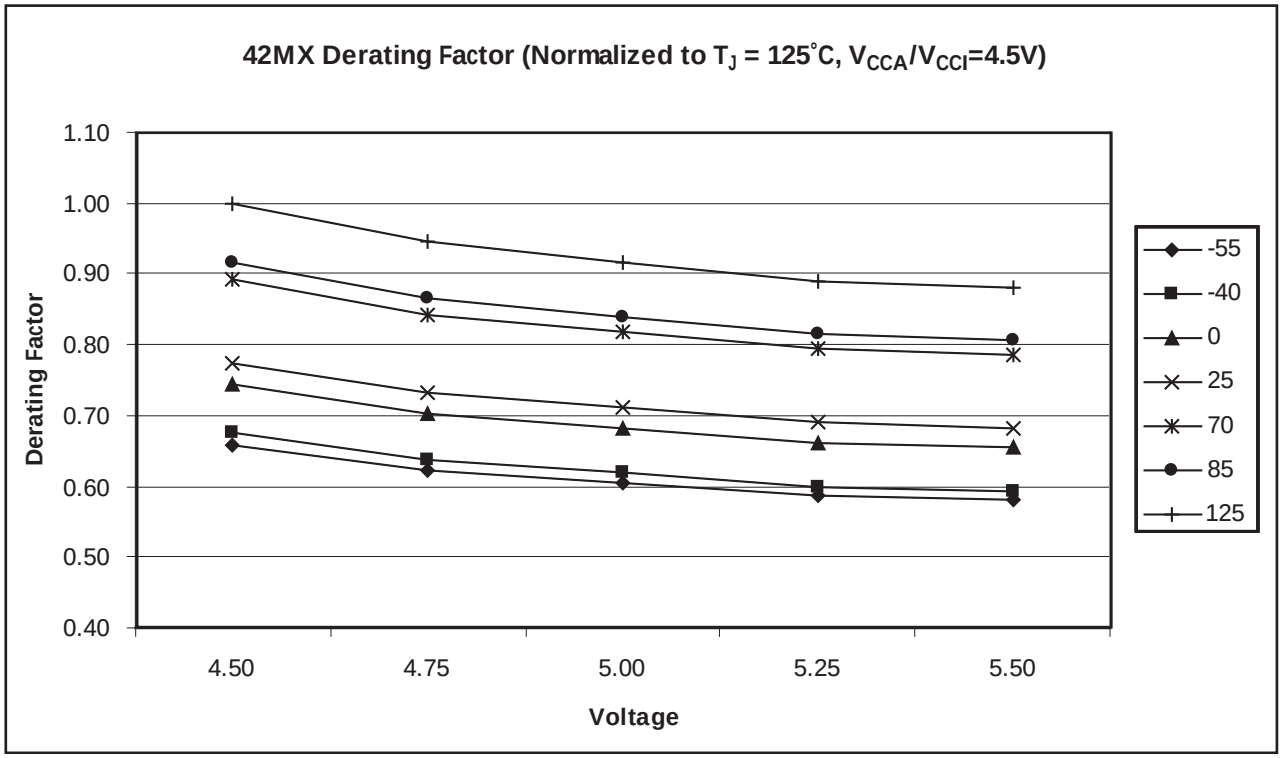
Long Tracks

Some nets in the design use long tracks, which are special routing resources that span multiple rows, columns, or modules. Long tracks employ three and sometimes four antifuse connections, which increase capacitance and resistance, resulting in longer net delays for macros connected to long tracks. Typically, up to 6 percent of nets in a fully utilized device require long tracks. Long tracks add approximately a 3 ns to a 6 ns delay, which is represented statistically in higher fanout (FO=8) routing delays in the data sheet specifications section, beginning on "Timing Information" on page 1-13.

Temperature and Voltage

Table 1-3 • **42MX Temperature and Voltage Derating Factors**
(Normalized to T_J = 125°C, V_{CCA}/V_{CCI} = 4.5V)

42MX Voltage	Temperature						
	–55°C	–40°C	0°C	25°C	70°C	85°C	125°C
4.50	0.66	0.67	0.74	0.78	0.89	0.91	1.00
4.75	0.62	0.64	0.70	0.73	0.84	0.86	0.94
5.00	0.60	0.62	0.68	0.71	0.82	0.84	0.92
5.25	0.59	0.60	0.66	0.69	0.79	0.81	0.89
5.50	0.58	0.59	0.66	0.68	0.79	0.81	0.88

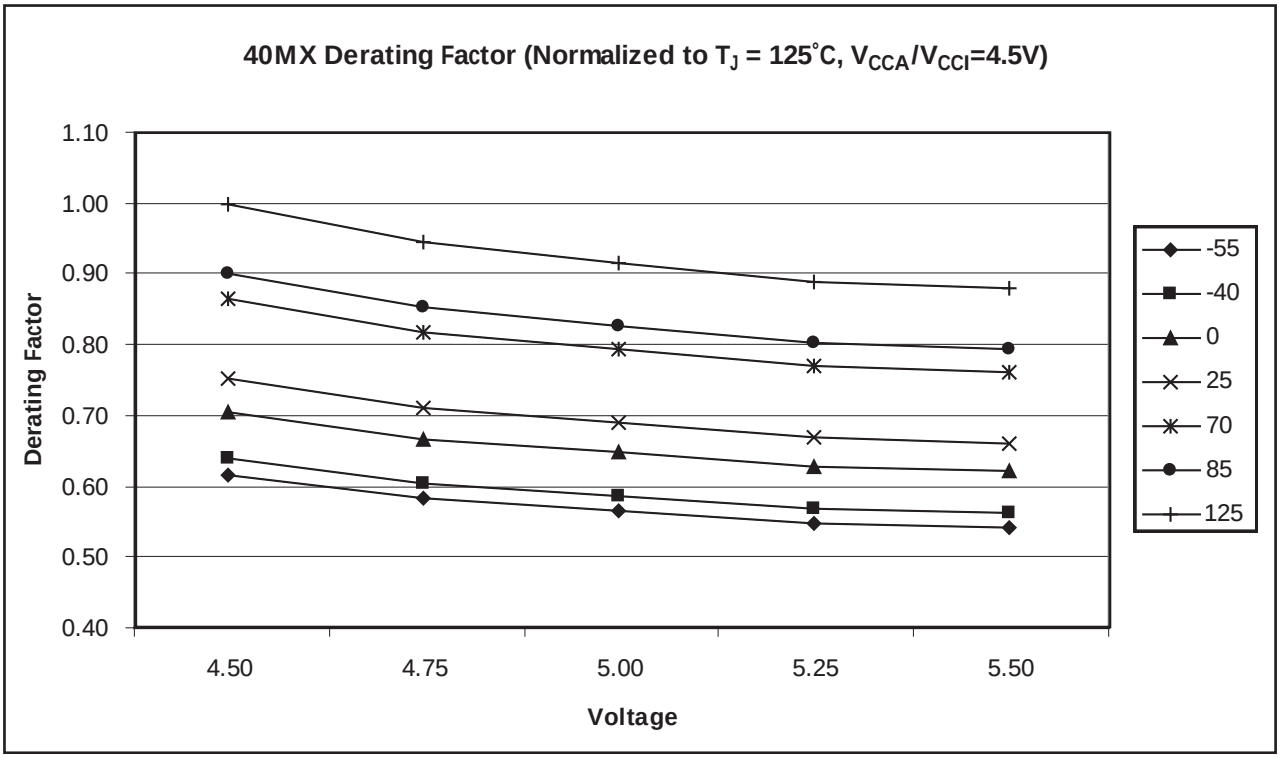


Note: *This derating factor applies to all routing and propagation delays.*

Figure 1-29 • **42MX Junction Temperature and Voltage Derating Curves**
(Normalized to T_J = 125°C, V_{CCA}/V_{CCI} = 4.5V)

Table 1-4 • **40MX Temperature and Voltage Derating Factors (Normalized to T_J = 125°C, V_{CC} = 4.5V)**

40MX Voltage	Temperature						
	–55°C	–40°C	0°C	25°C	70°C	85°C	125°C
4.50	0.62	0.64	0.71	0.75	0.86	0.90	1.00
4.75	0.58	0.60	0.67	0.71	0.82	0.85	0.94
5.00	0.57	0.59	0.65	0.69	0.79	0.83	0.92
5.25	0.55	0.57	0.63	0.67	0.77	0.80	0.89
5.50	0.54	0.56	0.62	0.66	0.76	0.79	0.88



Note: *This derating factor applies to all routing and propagation delays.*

Figure 1-30 • **40MX Junction Temperature and Voltage Derating Curves (Normalized to T_J = 125°C, V_{CCA}/V_{CCI} = 4.5V)**

Timing Characteristics

Table 1-5 • **A40MX02 Timing Characteristics (Nominal 5.0V Operation)**
Worst-Case Automotive Conditions, V_{CC} = 4.75V, T_J = 125°C

		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Units**
Logic Module Propagation Delays				
t_{PD1}	Single Module		2.3	ns
t_{PD2}	Dual-Module Macros		5.0	ns
t_{CO}	Sequential Clock-to-Q		2.3	ns
t_{GO}	Latch G-to-Q		2.3	ns
t_{RS}	Flip-Flop (Latch) Reset-to-Q		2.3	ns
Logic Module Predicted Routing Delays1				
t_{RD1}	FO=1 Routing Delay		2.5	ns
t_{RD2}	FO=2 Routing Delay		3.4	ns
t_{RD3}	FO=3 Routing Delay		4.4	ns
t_{RD4}	FO=4 Routing Delay		5.4	ns
t_{RD8}	FO=8 Routing Delay		9.3	ns
Logic Module Sequential Timing2				
t_{SUD}	Flip-Flop (Latch) Data Input Set-Up	5.8		ns
t_{HD}[3]	Flip-Flop (Latch) Data Input Hold	0.0		ns
t_{SUENA}	Flip-Flop (Latch) Enable Set-Up	5.8		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.0		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	6.1		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	6.1		ns
t_A	Flip-Flop Clock Input Period	9.2		ns
f_{MAX}	Flip-Flop (Latch) Clock Frequency (FO = 128)		163	MHz
Input Module Propagation Delays				
t_{INYH}	Pad-to-Y HIGH		1.4	ns
t_{INYL}	Pad-to-Y LOW		1.2	ns
Input Module Predicted Routing Delays1				
t_{IRD1}	FO=1 Routing Delay		3.9	ns
t_{IRD2}	FO=2 Routing Delay		4.9	ns
t_{IRD3}	FO=3 Routing Delay		5.9	ns
t_{IRD4}	FO=4 Routing Delay		6.9	ns
t_{IRD8}	FO=8 Routing Delay		10.8	ns

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
2. Set-up times assume fanout of 3. Further testing information can be obtained from the Timer utility.
3. The hold time for the DFME1A macro may be greater than 0 ns. Use the Series or later Timer to check the hold time for this macro.
4. Delays based on 35 pF loading.

Table 1-5 • **A40MX02 Timing Characteristics (Nominal 5.0V Operation)**
Worst-Case Automotive Conditions, V_{CC} = 4.75V, T_J = 125°C (Continued)

			'Std' Speed		
Parameter	**Description**		**Min.**	**Max.**	**Units**
Global Clock Network					
t_{CKH}	Input Low to HIGH	FO = 16 FO = 128		8.6 8.6	ns
t_{CKL}	Input High to LOW	FO = 16 FO = 128		9.1 9.1	ns
t_{PWH}	Minimum Pulse Width HIGH	FO = 16 FO = 128	4.2 4.4		ns
t_{PWL}	Minimum Pulse Width LOW	FO = 16 FO = 128	4.2 4.4		ns
t_{CKSW}	Maximum Skew	FO = 16 FO = 128		0.7 1.0	ns
t_P	Minimum Period	FO = 16 FO = 128	8.8 7.2		ns
f_{MAX}	Maximum Frequency	FO = 16 FO = 128		170 164	MHz
TTL Output Module Timing[4]					
t_{DLH}	Data-to-Pad HIGH			6.2	ns
t_{DHL}	Data-to-Pad LOW			7.5	ns
t_{ENZH}	Enable Pad Z to HIGH			7.1	ns
t_{ENZL}	Enable Pad Z to LOW			8.8	ns
t_{ENHZ}	Enable Pad HIGH to Z			14.9	ns
t_{ENLZ}	Enable Pad LOW to Z			11	ns
d_{TLH}	Delta LOW to HIGH			0.04	ns/pF
d_{THL}	Delta HIGH to LOW			0.05	ns/pF
CMOS Output Module Timing[4]					
t_{DLH}	Data-to-Pad HIGH			7.4	ns
t_{DHL}	Data-to-Pad LOW			6.4	ns
t_{ENZH}	Enable Pad Z to HIGH			6.4	ns
t_{ENZL}	Enable Pad Z to LOW			9.2	ns
t_{ENHZ}	Enable Pad HIGH to Z			14.9	ns
t_{ENLZ}	Enable Pad LOW to Z			11	ns
d_{TLH}	Delta LOW to HIGH			0.06	ns/pF
d_{THL}	Delta HIGH to LOW			0.04	ns/pF

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
2. Set-up times assume fanout of 3. Further testing information can be obtained from the Timer utility.
3. The hold time for the DFME1A macro may be greater than 0 ns. Use the Series or later Timer to check the hold time for this macro.
4. Delays based on 35 pF loading.

Table 1-6 • **A40MX04 Timing Characteristics (Nominal 5.0V Operation)**
Worst-Case Automotive Conditions, V_{CC} = 4.75V, T_J = 125°C

			'Std' Speed		
Parameter	**Description**		**Min.**	**Max.**	**Units**
Logic Module Propagation Delays					
t_{PD1}	Single Module			2.3	ns
t_{PD2}	Dual-Module Macros			5.0	ns
t_{CO}	Sequential Clock-to-Q			2.3	ns
t_{GO}	Latch G-to-Q			2.3	ns
t_{RS}	Flip-Flop (Latch) Reset-to-Q			2.3	ns
Logic Module Predicted Routing Delays[1]					
t_{RD1}	FO=1 Routing Delay			2.6	ns
t_{RD2}	FO=2 Routing Delay			3.6	ns
t_{RD3}	FO=3 Routing Delay			4.5	ns
t_{RD4}	FO=4 Routing Delay			5.5	ns
t_{RD8}	FO=8 Routing Delay			9.5	ns
Logic Module Sequential Timing[2]					
t_{SUD}	Flip-Flop (Latch) Data Input Set-Up		5.8		ns
t_{HD}[3]	Flip-Flop (Latch) Data Input Hold		0.0		ns
t_{SUENA}	Flip-Flop (Latch) Enable Set-Up		5.8		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold		0.0		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width		6.1		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width		6.2		ns
t_A	Flip-Flop Clock Input Period		9.2		ns
f_{MAX}	Flip-Flop (Latch) Clock Frequency	(FO = 128)		164	MHz
Input Module Propagation Delays					
t_{INYH}	Pad-to-Y HIGH			1.4	ns
t_{INYL}	Pad-to-Y LOW			1.2	ns
Input Module Predicted Routing Delays[1]					
t_{IRD1}	FO=1 Routing Delay			3.9	ns
t_{IRD2}	FO=2 Routing Delay			4.9	ns
t_{IRD3}	FO=3 Routing Delay			5.9	ns
t_{IRD4}	FO=4 Routing Delay			6.9	ns
t_{IRD8}	FO=8 Routing Delay			10.7	ns

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
2. Set-up times assume fanout of 3. Further testing information can be obtained from the Timer utility.
3. The hold time for the DFME1A macro may be greater than 0 ns. Use the Series or later Timer to check the hold time for this macro.
4. Delays based on 35 pF loading.

Table 1-6 • **A40MX04 Timing Characteristics (Nominal 5.0V Operation)**
Worst-Case Automotive Conditions, V_{CC} = 4.75V, T_J = 125°C (Continued)

			'Std' Speed		
Parameter	**Description**		**Min.**	**Max.**	**Units**
Global Clock Network					
t_{CKH}	Input LOW to HIGH	FO = 16 FO = 128		8.7 8.7	ns
t_{CKL}	Input HIGH to LOW	FO = 16 FO = 128		9.2 9.2	ns
t_{PWH}	Minimum Pulse Width HIGH	FO = 16 FO = 128	4.2 4.4		ns
t_{PWL}	Minimum Pulse Width LOW	FO = 16 FO = 128	4.2 4.2		ns
t_{CKSW}	Maximum Skew	FO = 16 FO = 128		0.7 1.0	ns
t_P	Minimum Period	FO = 16 FO = 128	8.8 9.2		ns
f_{MAX}	Maximum Frequency	FO = 16 FO = 128		170 164	MHz
TTL Output Module Timing[4]					
t_{DLH}	Data-to-Pad HIGH			6.2	ns
t_{DHL}	Data-to-Pad LOW			7.5	ns
t_{ENZH}	Enable Pad Z to HIGH			7.1	ns
t_{ENZL}	Enable Pad Z to LOW			8.8	ns
t_{ENHZ}	Enable Pad HIGH to Z			14.9	ns
t_{ENLZ}	Enable Pad LOW to Z			11	ns
d_{TLH}	Delta LOW to HIGH			0.04	ns/pF
d_{THL}	Delta HIGH to LOW			0.05	ns/pF
CMOS Output Module Timing[4]					
t_{DLH}	Data-to-Pad HIGH			7.5	ns
t_{DHL}	Data-to-Pad LOW			6.4	ns
t_{ENZH}	Enable Pad Z to HIGH			6.4	ns
t_{ENZL}	Enable Pad Z to LOW			9.2	ns
t_{ENHZ}	Enable Pad HIGH to Z			14.9	ns
t_{ENLZ}	Enable Pad LOW to Z			11	ns
d_{TLH}	Delta LOW to HIGH			0.07	ns/pF
d_{THL}	Delta HIGH to LOW			0.05	ns/pF

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
2. Set-up times assume fanout of 3. Further testing information can be obtained from the Timer utility.
3. The hold time for the DFME1A macro may be greater than 0 ns. Use the Series or later Timer to check the hold time for this macro.
4. Delays based on 35 pF loading.

Table 1-7 • **A42MX09 Timing Characteristics (Nominal 5.0V Operation)**
Worst-Case Automotive Conditions, V_{CC} = 4.75V, T_J = 125°C

		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Units**
Logic Module Propagation Delays[1]				
t_{PD1}	Single Module		2.1	ns
t_{CO}	Sequential Clock-to-Q		2.2	ns
t_{GO}	Latch G-to-Q		2.1	ns
t_{RS}	Flip-Flop (Latch) Reset-to-Q		2.5	ns
Logic Module Predicted Routing Delays[2]				
t_{RD1}	FO=1 Routing Delay		1.2	ns
t_{RD2}	FO=2 Routing Delay		1.7	ns
t_{RD3}	FO=3 Routing Delay		2.0	ns
t_{RD4}	FO=4 Routing Delay		2.4	ns
t_{RD8}	FO=8 Routing Delay		4.0	ns
Logic Module Sequential Timing[3, 4]				
t_{SUD}	Flip-Flop (Latch) Data Input Set-Up	0.6		ns
t_{HD}	Flip-Flop (Latch) Data Input Hold	0.0		ns
t_{SUENA}	Flip-Flop (Latch) Enable Set-Up	0.7		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.0		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	5.9		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	7.8		ns
t_A	Flip-Flop Clock Input Period	6.0		ns
t_{INH}	Input Buffer Latch Hold	0.0		ns
t_{INSU}	Input Buffer Latch Set-Up	0.5		ns
t_{OUTH}	Output Buffer Latch Hold	0.0		ns
t_{OUTSU}	Output Buffer Latch Set-Up	0.5		ns
f_{MAX}	Flip-Flop (Latch) Clock Frequency		229	MHz
Input Module Propagation Delays				
t_{INYH}	Pad-to-Y HIGH		1.9	ns
t_{INYL}	Pad-to-Y LOW		1.4	ns

1. For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
3. Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.
4. Set-up and hold timing parameters for the input buffer latch are defined with respect to the PAD and the D input. External setup/ hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.
5. Delays based on 35 pF loading.

Table 1-7 • **A42MX09 Timing Characteristics (Nominal 5.0V Operation)**
Worst-Case Automotive Conditions, V_{CC} = 4.75V, T_J = 125°C (Continued)

			'Std' Speed		
Parameter	**Description**		**Min.**	**Max.**	**Units**
t_{INGH}	G to Y HIGH			2.2	ns
t_{INGL}	G to Y LOW			2.2	ns
Input Module Predicted Routing Delays[2]					
t_{IRD1}	FO=1 Routing Delay			3.5	ns
t_{IRD2}	FO=2 Routing Delay			4.0	ns
t_{IRD3}	FO=3 Routing Delay			4.4	ns
t_{IRD4}	FO=4 Routing Delay			4.8	ns
t_{IRD8}	FO=8 Routing Delay			6.5	ns
Global Clock Network					
t_{CKH}	Input LOW to HIGH	FO = 32 FO = 256		4.2 4.7	ns ns
t_{CKL}	Input HIGH to LOW	FO = 32 FO = 256		6.1 6.7	ns ns
t_{PWH}	Minimum Pulse Width HIGH	FO = 32 FO = 256	2.1 2.4		ns ns
t_{PWL}	Minimum Pulse Width LOW	FO = 32 FO = 256	2.1 2.4		ns ns
t_{CKSW}	Maximum Skew	FO = 32 FO = 256		0.6 0.6	ns ns
t_{SUEXT}	Input Latch External Set-Up	FO = 32 FO = 256	0.0 0.0		ns ns
t_{HEXT}	Input Latch External Hold	FO = 32 FO = 256	4.1 4.6		ns ns
t_P	Minimum Period	FO = 32 FO = 256	5.5 6.1		ns ns
f_{MAX}	Maximum Frequency	FO = 32 FO = 256		253 229	MHz MHz
TTL Output Module Timing[5]					
t_{DLH}	Data-to-Pad HIGH			4.2	ns
t_{DHL}	Data-to-Pad LOW			5.1	ns
t_{ENZH}	Enable Pad Z to HIGH			4.6	ns

1. For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
3. Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.
4. Set-up and hold timing parameters for the input buffer latch are defined with respect to the PAD and the D input. External setup/ hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.
5. Delays based on 35 pF loading.

Table 1-7 • **A42MX09 Timing Characteristics (Nominal 5.0V Operation)**
Worst-Case Automotive Conditions, V_{CC} = 4.75V, T_J = 125°C (Continued)

		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Units**
t_{ENZL}	Enable Pad Z to LOW		5.1	ns
t_{ENHZ}	Enable Pad HIGH to Z		8.6	ns
t_{ENLZ}	Enable Pad LOW to Z		9.3	ns
t_{GLH}	G-to-Pad HIGH		4.5	ns
t_{GHL}	G-to-Pad LOW		4.5	ns
t_{LSU}	I/O Latch Set-Up	0.8		ns
t_{LH}	I/O Latch Hold	0.0		ns
t_{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad), 64 Clock Loading		9.1	ns
t_{ACO}	Array Clock-to-Out (Pad-to-Pad), 64 Clock Loading		12.8	ns
d_{TLH}	Capacity Loading, LOW to HIGH		0.05	ns/pF
d_{THL}	Capacity Loading, HIGH to LOW		0.06	ns/pF
CMOS Output Module Timing[5]				
t_{DLH}	Data-to-Pad HIGH		4.2	ns
t_{DHL}	Data-to-Pad LOW		5.1	ns
t_{ENZH}	Enable Pad Z to HIGH		4.6	ns
t_{ENZL}	Enable Pad Z to LOW		5.1	ns
t_{ENHZ}	Enable Pad HIGH to Z		8.6	ns
t_{ENLZ}	Enable Pad LOW to Z		9.3	ns
t_{GLH}	G-to-Pad HIGH		7.2	ns
t_{GHL}	G-to-Pad LOW		7.2	ns
t_{LSU}	I/O Latch Set-Up	0.8		ns
t_{LH}	I/O Latch Hold	0.0		ns
t_{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad), 64 Clock Loading		9.1	ns
t_{ACO}	Array Clock-to-Out (Pad-to-Pad), 64 Clock Loading		12.8	ns
d_{TLH}	Capacity Loading, LOW to HIGH		0.03	ns/pF
d_{THL}	Capacity Loading, HIGH to LOW		0.06	ns/pF

1. For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
3. Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.
4. Set-up and hold timing parameters for the input buffer latch are defined with respect to the PAD and the D input. External setup/ hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.
5. Delays based on 35 pF loading.

Table 1-8 • **A42MX16 Timing Characteristics (Nominal 5.0V Operation)**
Worst-Case Automotive Conditions, V_{CC} = 4.75V, T_J = 125°C

		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Units**
Logic Module Propagation Delays[1]				
t_{PD1}	Single Module		2.4	ns
t_{CO}	Sequential Clock-to-Q		2.5	ns
t_{GO}	Latch G-to-Q		2.4	ns
t_{RS}	Flip-Flop (Latch) Reset-to-Q		2.7	ns
Logic Module Predicted Routing Delays[2]				
t_{RD1}	FO=1 Routing Delay		1.4	ns
t_{RD2}	FO=2 Routing Delay		1.8	ns
t_{RD3}	FO=3 Routing Delay		2.2	ns
t_{RD4}	FO=4 Routing Delay		2.7	ns
t_{RD8}	FO=8 Routing Delay		4.5	ns
Logic Module Sequential Timing[3,4]				
t_{SUD}	Flip-Flop (Latch) Data Input Set-Up	0.6		ns
t_{HD}	Flip-Flop (Latch) Data Input Hold	0.0		ns
t_{SUENA}	Flip-Flop (Latch) Enable Set-Up	1.2		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.0		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	5.9		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	7.8		ns
t_A	Flip-Flop Clock Input Period	11.8		ns
t_{INH}	Input Buffer Latch Hold	0.0		ns
t_{INSU}	Input Buffer Latch Set-Up	0.8		ns
t_{OUTH}	Output Buffer Latch Hold	0.0		ns
t_{OUTSU}	Output Buffer Latch Set-Up	0.8		ns
f_{MAX}	Flip-Flop (Latch) Clock Frequency		1839.8	MHz
Input Module Propagation Delays				
t_{INYH}	Pad-to-Y HIGH		1.9	ns
t_{INYL}	Pad-to-Y LOW		1.5	ns

1. For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, point and position whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
3. Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.
4. Set-up and hold timing parameters for the input buffer latch are defined with respect to the PAD and the D input. External setup/ hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.
5. Delays based on 35 pF loading.

Table 1-8 • **A42MX16 Timing Characteristics (Nominal 5.0V Operation)**
Worst-Case Automotive Conditions, V_{CC} = 4.75V, T_J = 125°C (Continued)

			'Std' Speed		
Parameter	**Description**		**Min.**	**Max.**	**Units**
t_{INGH}	G to Y HIGH			2.5	ns
t_{INGL}	G to Y LOW			2.5	ns
Input Module Predicted Routing Delays2					
t_{IRD1}	FO=1 Routing Delay			3.2	ns
t_{IRD2}	FO=2 Routing Delay			3.6	ns
t_{IRD3}	FO=3 Routing Delay			4.1	ns
t_{IRD4}	FO=4 Routing Delay			4.6	ns
t_{IRD8}	FO=8 Routing Delay			6.3	ns
Global Clock Network					
t_{CKH}	Input LOW to HIGH	FO = 32 FO = 384		4.6 5.1	ns ns
t_{CKL}	Input HIGH to LOW	FO = 32 FO = 384		6.6 7.8	ns ns
t_{PWH}	Minimum Pulse Width HIGH	FO = 32 FO = 384	5.5 6.3		ns ns
t_{PWL}	Minimum Pulse Width LOW	FO = 32 FO = 384	5.5 6.3		ns ns
t_{CKSW}	Maximum Skew	FO = 32 FO = 384		0.6 0.6	ns ns
t_{SUEXT}	Input Latch External Set-Up	FO = 32 FO = 384	0.0 0.0		ns ns
t_{HEXT}	Input Latch External Hold	FO = 32 FO = 384	4.8 5.5		ns ns
t_P	Minimum Period	FO = 32 FO = 384	6.8 7.5		ns ns
f_{MAX}	Maximum Frequency	FO = 32 FO = 384		202 183	MHz MHz
TTL Output Module Timing5					
t_{DLH}	Data-to-Pad HIGH			4.4	ns
t_{DHL}	Data-to-Pad LOW			5.2	ns

1. For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, point and position whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
3. Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.
4. Set-up and hold timing parameters for the input buffer latch are defined with respect to the PAD and the D input. External setup/ hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.
5. Delays based on 35 pF loading.

Table 1-8 • **A42MX16 Timing Characteristics (Nominal 5.0V Operation)**
Worst-Case Automotive Conditions, V_{CC} = 4.75V, T_J = 125°C (Continued)

		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Units**
t_{ENZH}	Enable Pad Z to HIGH		4.7	ns
t_{ENZL}	Enable Pad Z to LOW		5.2	ns
t_{ENHZ}	Enable Pad HIGH to Z		9.4	ns
t_{ENLZ}	Enable Pad LOW to Z		8.7	ns
t_{GLH}	G-to-Pad HIGH		5.1	ns
t_{GHL}	G-to-Pad LOW		5.1	ns
t_{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad), 64 Clock Loading		9.9	ns
t_{ACO}	Array Clock-to-Out (Pad-to-Pad), 64 Clock Loading		14	ns
d_{TLH}	Capacitive Loading, LOW to HIGH		0.05	ns/pF
d_{THL}	Capacitive Loading, HIGH to LOW		0.06	ns/pF
CMOS Output Module Timing[5]				
t_{DLH}	Data-to-Pad HIGH		5.5	ns
t_{DHL}	Data-to-Pad LOW		4.2	ns
t_{ENZH}	Enable Pad Z to HIGH		4.7	ns
t_{ENZL}	Enable Pad Z to LOW		5.2	ns
t_{ENHZ}	Enable Pad HIGH to Z		9.4	ns
t_{ENLZ}	Enable Pad LOW to Z		8.7	ns
t_{GLH}	G-to-Pad HIGH		8.8	ns
t_{GHL}	G-to-Pad LOW		8.8	ns
t_{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad), 64 Clock Loading		9.9	ns
t_{ACO}	Array Clock-to-Out (Pad-to-Pad), 64 Clock Loading		14	ns
d_{TLH}	Capacitive Loading, LOW to HIGH		0.05	ns/pF
d_{THL}	Capacitive Loading, HIGH to LOW		0.06	ns/pF

1. For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, point and position whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
3. Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.
4. Set-up and hold timing parameters for the input buffer latch are defined with respect to the PAD and the D input. External setup/ hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.
5. Delays based on 35 pF loading.

Table 1-9 • **A42MX24 Timing Characteristics (Nominal 5.0V Operation)**
Worst-Case Automotive Conditions, V_{CC} = 4.75V, T_J = 125°C

		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Units**
Logic Module Combinatorial Functions[1]				
t_{PD}	Internal Array Module Delay		2.1	ns
t_{PDD}	Internal Decode Module Delay		2.5	ns
Logic Module Predicted Routing Delays[2]				
t_{RD1}	FO=1 Routing Delay		1.4	ns
t_{RD2}	FO=2 Routing Delay		1.7	ns
t_{RD3}	FO=3 Routing Delay		2.2	ns
t_{RD4}	FO=4 Routing Delay		2.6	ns
t_{RD5}	FO=8 Routing Delay		4.2	ns
Logic Module Sequential Timing[3, 4]				
t_{CO}	Flip-Flop Clock-to-Output		2.2	ns
t_{GO}	Latch Gate-to-Output		2.1	ns
t_{SU}	Flip-Flop (Latch) Set-Up Time	0.6		ns
t_{H}	Flip-Flop (Latch) Hold Time	0.0		ns
t_{RO}	Flip-Flop (Latch) Reset-to-Output		2.5	ns
t_{SUENA}	Flip-Flop (Latch) Enable Set-Up	0.7		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.0		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	5.8		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	7.6		ns
Input Module Propagation Delays				
t_{INPY}	Input Data Pad-to-Y		1.8	ns
t_{INGO}	Input Latch Gate-to-Output		2.2	ns
t_{INH}	Input Latch Hold	0.0		ns
t_{INSU}	Input Latch Set-Up	0.8		ns
t_{ILA}	Latch Active Pulse Width	8.1		ns
Input Module Predicted Routing Delays[2]				
t_{IRD1}	FO=1 Routing Delay		3.2	ns

1. For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
3. Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.
4. Set-up and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/ hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.
5. Delays based on 35 pF loading.

Table 1-9 • **A42MX24 Timing Characteristics (Nominal 5.0V Operation)**
Worst-Case Automotive Conditions, V_{CC} = 4.75V, T_J = 125°C (Continued)

			'Std' Speed		
Parameter	**Description**		**Min.**	**Max.**	**Units**
t_{IRD2}	FO=2 Routing Delay			3.6	ns
t_{IRD3}	FO=3 Routing Delay			4.0	ns
t_{IRD4}	FO=4 Routing Delay			4.3	ns
t_{IRD8}	FO=8 Routing Delay			6.0	ns
Global Clock Network					
t_{CKH}	Input LOW to HIGH	FO=32 FO=486		4.6 5.1	ns ns
t_{CKL}	Input HIGH to LOW	FO=32 FO=486		6.3 7.4	ns ns
t_{PWH}	Minimum Pulse Width HIGH	FO=32 FO=486	3.8 4.1		ns ns
t_{PWL}	Minimum Pulse Width LOW	FO=32 FO=486	3.8 4.1		ns ns
t_{CKSW}	Maximum Skew	FO=32 FO=486		0.9 0.9	ns ns
t_{SUEXT}	Input Latch External Set-Up	FO=32 FO=486	0.0 0.0		ns ns
t_{HEXT}	Input Latch External Hold	FO=32 FO=486	4.8 5.8		ns ns
t_P	Minimum Period ($1/f_{MAX}$)	FO=32 FO=486	7.6 8.4		ns ns
f_{MAX}	Maximum Datapath Frequency	FO=32 FO=486		180 165	MHz MHz
TTL Output Module Timing5					
t_{DLH}	Data-to-Pad HIGH			4.2	ns
t_{DHL}	Data-to-Pad LOW			4.9	ns
t_{ENZH}	Enable Pad Z to HIGH			4.5	ns
t_{ENZL}	Enable Pad Z to LOW			4.9	ns
t_{ENHZ}	Enable Pad HIGH to Z			8.9	ns
t_{ENLZ}	Enable Pad LOW to Z			8.3	ns
t_{GLH}	G-to-Pad HIGH			5.1	ns

1. For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
3. Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.
4. Set-up and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/ hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.
5. Delays based on 35 pF loading.

Table 1-9 • **A42MX24 Timing Characteristics (Nominal 5.0V Operation)**
Worst-Case Automotive Conditions, V_{CC} = 4.75V, T_J = 125°C (Continued)

		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Units**
t_{GHL}	G-to-Pad LOW		5.1	ns
t_{LSU}	I/O Latch Output Set-Up	0.8		ns
t_{LH}	I/O Latch Output Hold	0.0		ns
t_{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O		9.5	ns
t_{ACO}	Array Latch Clock-to-Out (Pad-to-Pad) 32 I/O		18.5	ns
d_{TLH}	Capacitive Loading, LOW to HIGH		0.06	ns/pF
d_{THL}	Capacitive Loading, HIGH to LOW		0.05	ns/pF
CMOS Output Module Timing[5]				
t_{DLH}	Data-to-Pad HIGH		5.1	ns
t_{DHL}	Data-to-Pad LOW		4.1	ns
t_{ENZH}	Enable Pad Z to HIGH		4.1	ns
t_{ENZL}	Enable Pad Z to LOW		4.9	ns
t_{ENHZ}	Enable Pad HIGH to Z		8.9	ns
t_{ENLZ}	Enable Pad LOW to Z		8.3	ns
t_{GLH}	G-to-Pad HIGH		8.5	ns
t_{GHL}	G-to-Pad LOW		8.5	ns
t_{LSU}	I/O Latch Set-Up	0.8		ns
t_{LH}	I/O Latch Hold	0.0		ns
t_{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O		9.5	ns
t_{ACO}	Array Latch Clock-to-Out (Pad-to-Pad) 32 I/O		18.5	ns
d_{TLH}	Capacitive Loading, LOW to HIGH		0.06	ns/pF
d_{THL}	Capacitive Loading, HIGH to LOW		0.05	ns/pF

1. For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
3. Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.
4. Set-up and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/ hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.
5. Delays based on 35 pF loading.

Table 1-10 • **A42MX36 Timing Characteristics (Nominal 5.0V Operation)**
Worst-Case Automotive Conditions, V_{CC} = 4.75V, T_J = 125°C

		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Units**
Logic Module Combinatorial Functions[1]				
t_{PD}	Internal Array Module Delay		2.4	ns
t_{PDD}	Internal Decode Module Delay		2.8	ns
Logic Module Predicted Routing Delays[2]				
t_{RD1}	FO=1 Routing Delay		1.6	ns
t_{RD2}	FO=2 Routing Delay		2.2	ns
t_{RD3}	FO=3 Routing Delay		2.8	ns
t_{RD4}	FO=4 Routing Delay		3.4	ns
t_{RD5}	FO=8 Routing Delay		5.8	ns
t_{RDD}	Decode-to-Output Routing Delay		0.6	ns
Logic Module Sequential Timing[3, 4]				
t_{CO}	Flip-Flop Clock-to-Output		2.2	ns
t_{GO}	Latch Gate-to-Output		2.2	ns
t_{SU}	Flip-Flop (Latch) Set-Up Time	0.6		ns
t_{H}	Flip-Flop (Latch) Hold Time	0.0		ns
t_{RO}	Flip-Flop (Latch) Reset-to-Output		2.7	ns
t_{SUENA}	Flip-Flop (Latch) Enable Set-Up	1.2		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.0		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	5.8		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	7.5		ns
Synchronous SRAM Operations				
t_{RC}	Read Cycle Time	11.8		ns
t_{WC}	Write Cycle Time	11.8		ns
t_{RCKHL}	Clock HIGH/LOW Time	5.9		ns
t_{RCO}	Data Valid After Clock HIGH/LOW		5.9	ns
t_{ADSU}	Address/Data Set-Up Time	2.8		ns
t_{ADH}	Address/Data Hold Time	0.0		ns

1. For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
3. Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.
4. Set-up and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.
5. Delays based on 35 pF loading.

Table 1-10 • **A42MX36 Timing Characteristics (Nominal 5.0V Operation)**
Worst-Case Automotive Conditions, V_{CC} = 4.75V, T_J = 125°C (Continued)

		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Units**
t_{RENSU}	Read Enable Set-Up	1.1		ns
t_{RENH}	Read Enable Hold	5.9		ns
t_{WENSU}	Write Enable Set-Up	4.7		ns
t_{WENH}	Write Enable Hold	0.0		ns
t_{BENS}	Block Enable Set-Up	4.8		ns
t_{BENH}	Block Enable Hold	0.0		ns
Asynchronous SRAM Operations				
t_{RPD}	Asynchronous Access Time		14.1	ns
t_{RDADV}	Read Address Valid	15.3		ns
t_{ADSU}	Address/Data Set-Up Time	2.9		ns
t_{ADH}	Address/Data Hold Time	0.0		ns
t_{RENSUA}	Read Enable Set-Up to Address Valid	1.1		ns
t_{RENHA}	Read Enable Hold	5.9		ns
t_{WENSU}	Write Enable Set-Up	4.7		ns
t_{WENH}	Write Enable Hold	0.0		ns
t_{DOH}	Data Out Hold Time		2.1	ns
Input Module Propagation Delays				
t_{INPY}	Input Data Pad-to-Y		1.8	ns
t_{INGO}	Input Latch Gate-to-Output		2.5	ns
t_{INH}	Input Latch Hold	0.0		ns
t_{INSU}	Input Latch Set-Up	0.8		ns
t_{ILA}	Latch Active Pulse Width	8.1		ns
Input Module Predicted Routing Delays[2]				
t_{IRD1}	FO=1 Routing Delay		3.4	ns
t_{IRD2}	FO=2 Routing Delay		4.0	ns
t_{IRD3}	FO=3 Routing Delay		4.6	ns
t_{IRD4}	FO=4 Routing Delay		5.2	ns

1. For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
3. Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.
4. Set-up and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.
5. Delays based on 35 pF loading.

Table 1-10 • **A42MX36 Timing Characteristics (Nominal 5.0V Operation)**
Worst-Case Automotive Conditions, V_{CC} = 4.75V, T_J = 125°C (Continued)

			'Std' Speed		
Parameter	**Description**		**Min.**	**Max.**	**Units**
t_{IRD8}	FO=8 Routing Delay			7.5	ns
Global Clock Network					
t_{CKH}	Input LOW to HIGH	FO=32 FO=635		4.7 5.2	ns ns
t_{CKL}	Input HIGH to LOW	FO=32 FO=635		6.6 8.5	ns ns
t_{PWH}	Minimum Pulse Width HIGH	FO=32 FO=635	3.1 3.4		ns ns
t_{PWL}	Minimum Pulse Width LOW	FO=32 FO=635	3.1 3.4		ns ns
t_{CKSW}	Maximum Skew	FO=32 FO=635		1.2 1.2	ns ns
t_{SUEXT}	Input Latch External Set-Up	FO=32 FO=635	0.0 0.0		ns ns
t_{HEXT}	Input Latch External Hold	FO=32 FO=635	4.9 5.8		ns ns
t_P	Minimum Period ($1/f_{MAX}$)	FO=32 FO=635	8.9 9.8		ns ns
f_{HMAX}	Maximum Datapath Frequency	FO=32 FO=635		154 142	MHz MHz
TTL Output Module Timing[1]					
t_{DLH}	Data-to-Pad HIGH			4.5	ns
t_{DHL}	Data-to-Pad LOW			5.2	ns
t_{ENZH}	Enable Pad Z to HIGH			4.6	ns
t_{ENZL}	Enable Pad Z to LOW			5.1	ns
t_{ENHZ}	Enable Pad HIGH to Z			9.2	ns
t_{ENLZ}	Enable Pad LOW to Z			8.6	ns
t_{GLH}	G-to-Pad HIGH			5.2	ns
t_{GHL}	G-to-Pad LOW			5.2	ns
t_{LSU}	I/O Latch Output Set-Up		0.8		ns
t_{LH}	I/O Latch Output Hold		0.0		ns

1. For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
3. Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.
4. Set-up and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.
5. Delays based on 35 pF loading.

Table 1-10 • **A42MX36 Timing Characteristics (Nominal 5.0V Operation)**
Worst-Case Automotive Conditions, V_{CC} = 4.75V, T_J = 125°C (Continued)

		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Units**
t_{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O		8.4	ns
t_{ACO}	Array Latch Clock-to-Out (Pad-to-Pad) 32 I/O		11.5	ns
d_{TLH}	Capacitive Loading, LOW to HIGH		0.10	ns/pF
d_{THL}	Capacitive Loading, HIGH to LOW		0.10	ns/pF
CMOS Output Module Timing[5]				
t_{DLH}	Data-to-Pad HIGH		6.1	ns
t_{DHL}	Data-to-Pad LOW		4.2	ns
t_{ENZH}	Enable Pad Z to HIGH		4.6	ns
t_{ENZL}	Enable Pad Z to LOW		5.1	ns
t_{ENHZ}	Enable Pad HIGH to Z		9.2	ns
t_{ENLZ}	Enable Pad LOW to Z		8.6	ns
t_{GLH}	G-to-Pad HIGH		8.8	ns
t_{GHL}	G-to-Pad LOW		8.8	ns
t_{LSU}	I/O Latch Set-Up	0.8		ns
t_{LH}	I/O Latch Hold	0.0		ns
t_{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O		9.9	ns
t_{ACO}	Array Latch Clock-to-Out (Pad-to-Pad) 32 I/O		13.5	ns
d_{TLH}	Capacitive Loading, LOW to HIGH		0.12	ns/pF
d_{THL}	Capacitive Loading, HIGH to LOW		0.12	ns/pF

1. For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
3. Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.
4. Set-up and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.
5. Delays based on 35 pF loading.

Pin Descriptions

CLK, CLKA,B, I/O Global Clock (Input)

TTL clock inputs for clock distribution networks. The clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

DCLK, I/O Diagnostic Clock (Input)

TTL clock input for diagnostic probe and device programming. DCLK is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

GND Ground (Input)

Input LOW supply voltage.

I/O Input/Output (Input, Output)

Input, output, tri-state, or bi-directional buffer. Input and output levels are compatible with standard TTL and CMOS specifications. Unused I/O pins are automatically driven LOW by the Designer Series software.

MODE Mode (Input)

Controls the use of multifunction pins (DCLK, PRA, PRB, SDI, TDO). To provide verification capability, the MODE pin should be held HIGH. To facilitate this, the MODE pin should be tied to GND through a 10KΩ resistor so that the MODE pin can be pulled HIGH when required.

NC No Connection

This pin is not connected to circuitry within the device. These pins can be driven to any voltage or can be left floating with no effect on the operation of the device.

PRA, PRB, I/O Probe

The pins are used for real-time diagnostic output of any signal path within the device. Each pin can be used as a user-defined I/O when verification has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality. PRA and PRB are accessible when the MODE pin is HIGH. These pins function as I/Os when the MODE pin is LOW.

QCLKA,B,C,D, I/O Quadrant Clock (Input/Output)

Quadrant clock inputs. When not used as a register control signal, these pins can function as general-purpose I/Os.

SDI, I/O Serial Data Input

Serial data input for diagnostic probe and device programming. SDI is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

SDO, TDO, I/O Serial Data Output

Serial data output for diagnostic probe and device programming. SDO is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW. SDO is not available for 40MX devices.

TCK, I/O Test Clock

Clock signal to shift the Boundary Scan Test (BST) data into the device. This pin functions as an I/O when the test fuse is not programmed. BST pins are only available in the A42MX24 and A42MX36 devices.

TDI, I/O Test Data In

Serial data input for BST instructions and data. Data is shifted in on the rising edge of TCK. This pin functions as an I/O when the test fuse is not programmed. BST pins are only available in the A42MX24 and A42MX36 devices.

TDO, I/O Test Data Out

Serial data output for BST instructions and test data. This pin functions as an I/O when the test fuse is not programmed. BST pins are only available in the A42MX24 and A42MX36 devices.

TMS, I/O Test Mode Select

Serial data input for boundary scan test mode. Data is shifted in on the rising edge of TCK. This pin functions as an I/O when the test fuse is not programmed. BST pins are only available in the A42MX24 and A42MX36 devices.

V_{CC} Supply Voltage Input

Input HIGH supply voltage for 40 MX devices.

V_{CCA} Supply Voltage Input

Input HIGH supply voltage, supplies array core for 42MX devices.

V_{CCI} Supply Voltage Input

Input HIGH supply voltage, supplies I/O cells only for 42MX devices.

WD, I/O Wide Decode Output

When a wide decode module is used in a 42MX device, this pin can be used as a dedicated output from the wide decode module. This direct connection eliminates additional interconnect delays associated with regular logic modules. To implement the direct I/O connection, connect an output buffer of any type to the output of the wide decode macro and place this output on one of the reserved WD pins. When a wide decode module is not used, this pin functions as a regular I/O pin.

Package Pin Assignments

68-Pin PLCC

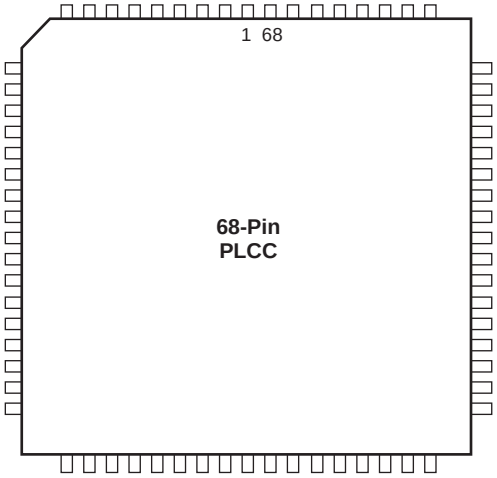


Figure 2-1 • **68-Pin PLCC**

68-Pin PLCC	
Pin Number	**A40MX02 Function**
1	I/O
2	I/O
3	I/O
4	V_{CC}
5	I/O
6	I/O
7	I/O
8	I/O
9	I/O
10	I/O
11	I/O
12	I/O
13	I/O
14	GND
15	GND
16	I/O
17	I/O
18	I/O

68-Pin PLCC	
Pin Number	**A40MX02 Function**
19	I/O
20	I/O
21	V_{CC}
22	I/O
23	I/O
24	I/O
25	V_{CC}
26	I/O
27	I/O
28	I/O
29	I/O
30	I/O
31	I/O
32	GND
33	I/O
34	I/O
35	I/O
36	I/O

68-Pin PLCC	
Pin Number	**A40MX02 Function**
37	I/O
38	V_{CC}
39	I/O
40	I/O
41	I/O
42	I/O
43	I/O
44	I/O
45	I/O
46	I/O
47	I/O
48	I/O
49	GND
50	I/O
51	I/O
52	CLK, I/O
53	I/O
54	MODE

68-Pin PLCC	
Pin Number	**A40MX02 Function**
55	V_{CC}
56	SDI, I/O
57	DCLK, I/O
58	PRA, I/O
59	PRB, I/O
60	I/O
61	I/O
62	I/O
63	I/O
64	I/O
65	I/O
66	GND
67	I/O
68	I/O

84-Pin PLCC

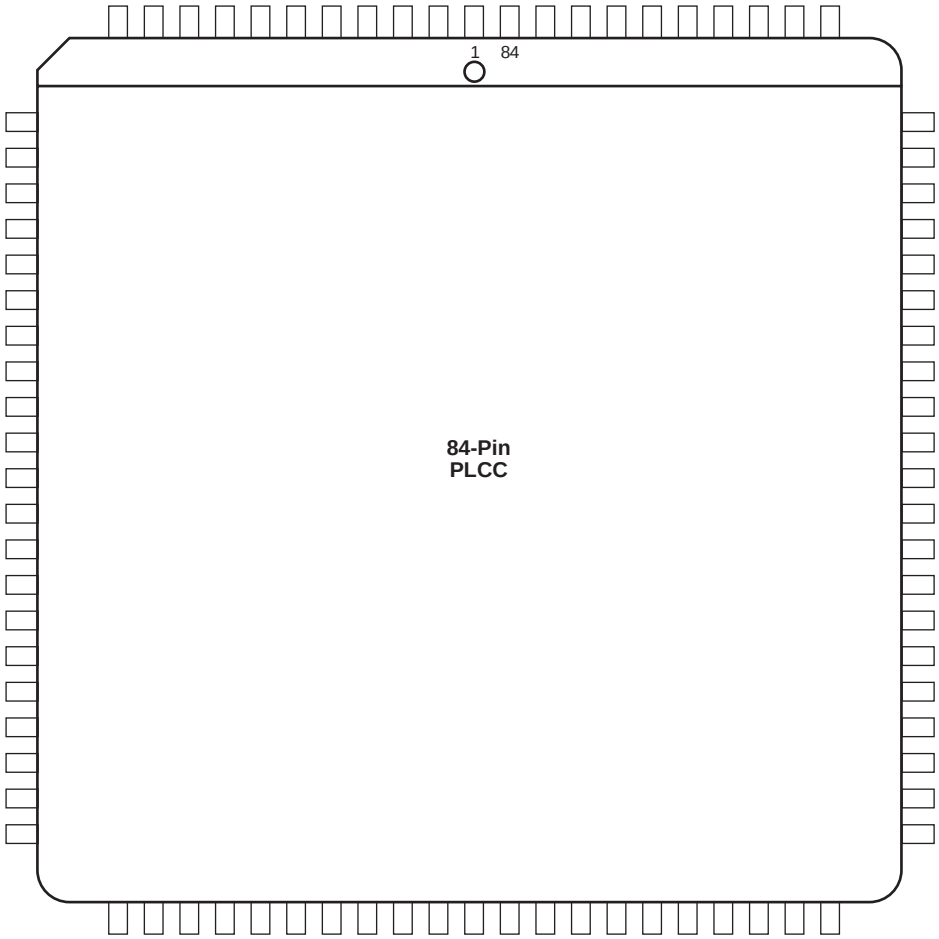


Figure 2-2 • **84-Pin PLCC**

84-Pin PLCC		
Pin Number	A40MX04 Function	A42MX09 Function
1	I/O	I/O
2	I/O	CLKB, I/O
3	I/O	I/O
4	V_{CC}	PRB, I/O
5	I/O	I/O
6	I/O	GND
7	I/O	I/O
8	I/O	I/O
9	I/O	I/O
10	I/O	DCLK, I/O
11	I/O	I/O
12	NC	MODE
13	I/O	I/O
14	I/O	I/O
15	I/O	I/O
16	I/O	I/O
17	I/O	I/O
18	GND	I/O
19	GND	I/O
20	I/O	I/O
21	I/O	I/O
22	I/O	V_{CCA}
23	I/O	V_{CCI}
24	I/O	I/O
25	V_{CC}	I/O
26	V_{CC}	I/O
27	I/O	I/O
28	I/O	GND
29	I/O	I/O
30	I/O	I/O
31	I/O	I/O
32	I/O	I/O
33	V_{CC}	I/O
34	I/O	I/O
35	I/O	I/O

84-Pin PLCC		
Pin Number	A40MX04 Function	A42MX09 Function
36	I/O	I/O
37	I/O	I/O
38	I/O	I/O
39	I/O	I/O
40	GND	I/O
41	I/O	I/O
42	I/O	I/O
43	I/O	V_{CCA}
44	I/O	I/O
45	I/O	I/O
46	V_{CC}	I/O
47	I/O	I/O
48	I/O	I/O
49	I/O	GND
50	I/O	I/O
51	I/O	I/O
52	I/O	SDO, I/O
53	I/O	I/O
54	I/O	I/O
55	I/O	I/O
56	I/O	I/O
57	I/O	I/O
58	I/O	I/O
59	I/O	I/O
60	GND	I/O
61	GND	I/O
62	I/O	I/O
63	I/O	GND
64	CLK, I/O	V_{CCA}
65	I/O	V_{CCI}
66	MODE	I/O
67	V_{CC}	I/O
68	V_{CC}	I/O
69	I/O	I/O
70	I/O	GND

84-Pin PLCC		
Pin Number	A40MX04 Function	A42MX09 Function
71	I/O	I/O
72	SDI, I/O	I/O
73	DCLK, I/O	I/O
74	PRA, I/O	I/O
75	PRB, I/O	I/O
76	I/O	SDI, I/O
77	I/O	I/O
78	I/O	I/O
79	I/O	I/O
80	I/O	I/O
81	I/O	PRA, I/O
82	GND	I/O
83	I/O	CLKA, I/O
84	I/O	V_{CCA}

100-Pin PQFP Package (Top View)

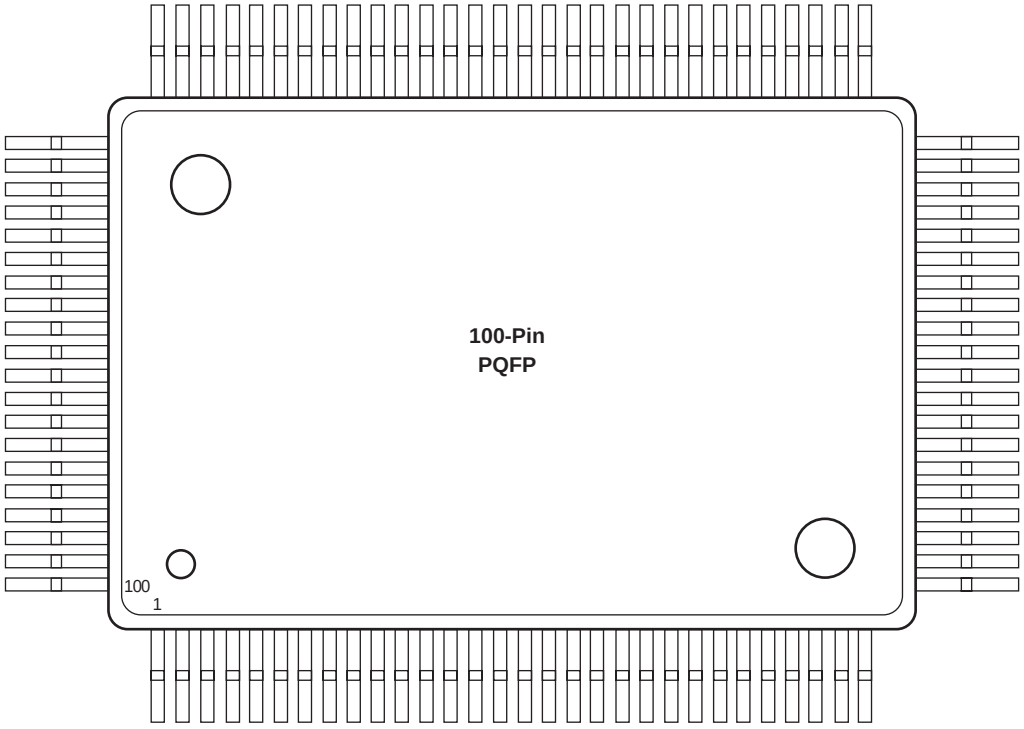


Figure 2-3 • **100-Pin PQFP**

100-Pin PQFP			
Pin Number	**A40MX02 Function**	**A40MX04 Function**	**A42MX09 Function**
1	NC	NC	I/O
2	NC	NC	DCLK, I/O
3	NC	NC	I/O
4	NC	NC	MODE
5	NC	NC	I/O
6	PRB, I/O	PRB, I/O	I/O
7	I/O	I/O	I/O
8	I/O	I/O	I/O
9	I/O	I/O	GND
10	I/O	I/O	I/O
11	I/O	I/O	I/O
12	I/O	I/O	I/O
13	GND	GND	I/O
14	I/O	I/O	I/O
15	I/O	I/O	I/O
16	I/O	I/O	V_{CCA}
17	I/O	I/O	V_{CCI}
18	I/O	I/O	I/O
19	V_{CC}	V_{CC}	I/O
20	I/O	I/O	I/O
21	I/O	I/O	I/O
22	I/O	I/O	GND
23	I/O	I/O	I/O
24	I/O	I/O	I/O
25	I/O	I/O	I/O
26	I/O	I/O	I/O
27	NC	NC	I/O
28	NC	NC	I/O
29	NC	NC	I/O
30	NC	NC	I/O
31	NC	I/O	I/O
32	NC	I/O	I/O
33	NC	I/O	I/O
34	I/O	I/O	GND
35	I/O	I/O	I/O

100-Pin PQFP			
Pin Number	**A40MX02 Function**	**A40MX04 Function**	**A42MX09 Function**
36	GND	GND	I/O
37	GND	GND	I/O
38	I/O	I/O	I/O
39	I/O	I/O	I/O
40	I/O	I/O	V_{CCA}
41	I/O	I/O	I/O
42	I/O	I/O	I/O
43	V_{CC}	V_{CC}	I/O
44	V_{CC}	V_{CC}	I/O
45	I/O	I/O	I/O
46	I/O	I/O	GND
47	I/O	I/O	I/O
48	NC	I/O	I/O
49	NC	I/O	I/O
50	NC	I/O	I/O
51	NC	NC	I/O
52	NC	NC	SDO, I/O
53	NC	NC	I/O
54	NC	NC	I/O
55	NC	NC	I/O
56	V_{CC}	V_{CC}	I/O
57	I/O	I/O	GND
58	I/O	I/O	I/O
59	I/O	I/O	I/O
60	I/O	I/O	I/O
61	I/O	I/O	I/O
62	I/O	I/O	I/O
63	GND	GND	I/O
64	I/O	I/O	GND
65	I/O	I/O	V_{CCA}
66	I/O	I/O	V_{CCI}
67	I/O	I/O	V_{CCA}
68	I/O	I/O	I/O
69	V_{CC}	V_{CC}	I/O
70	I/O	I/O	I/O

100-Pin PQFP			
Pin Number	**A40MX02 Function**	**A40MX04 Function**	**A42MX09 Function**
71	I/O	I/O	I/O
72	I/O	I/O	GND
73	I/O	I/O	I/O
74	I/O	I/O	I/O
75	I/O	I/O	I/O
76	I/O	I/O	I/O
77	NC	NC	I/O
78	NC	NC	I/O
79	NC	NC	SDI, I/O
80	NC	I/O	I/O
81	NC	I/O	I/O
82	NC	I/O	I/O
83	I/O	I/O	I/O
84	I/O	I/O	GND
85	I/O	I/O	I/O
86	GND	GND	I/O
87	GND	GND	PRA, I/O
88	I/O	I/O	I/O
89	I/O	I/O	CLKA, I/O
90	CLK, I/O	CLK, I/O	V_{CCA}
91	I/O	I/O	I/O
92	MODE	MODE	CLKB, I/O
93	V_{CC}	V_{CC}	I/O
94	V_{CC}	V_{CC}	PRB, I/O
95	NC	I/O	I/O
96	NC	I/O	GND
97	NC	I/O	I/O
98	SDI, I/O	SDI, I/O	I/O
99	DCLK, I/O	DCLK, I/O	I/O
100	PRA, I/O	PRA, I/O	I/O

160-Pin PQFP Package (Top View)

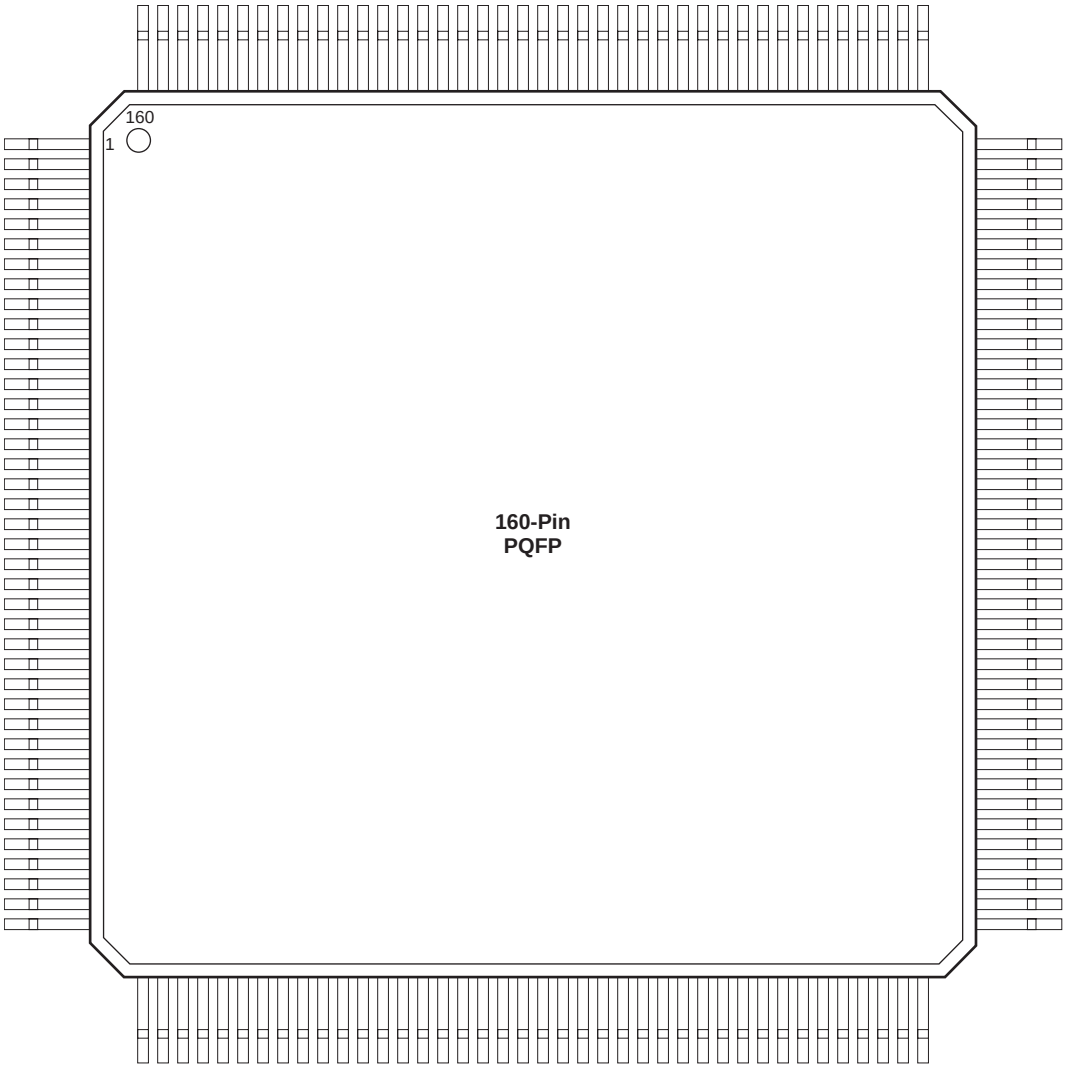


Figure 2-4 • **Pin PQFP**

160-Pin PQFP		
Pin Number	**A42MX09 Function**	**A42MX24 Function**
1	I/O	I/O
2	DCLK, I/O	DCLK, I/O
3	NC	I/O
4	I/O	WD, I/O
5	I/O	WD, I/O
6	NC	V_{CCI}
7	I/O	I/O
8	I/O	I/O
9	I/O	I/O
10	NC	I/O
11	GND	GND
12	NC	I/O
13	I/O	WD, I/O
14	I/O	WD, I/O
15	I/O	I/O
16	PRB, I/O	PRB, I/O
17	I/O	I/O
18	CLKB, I/O	CLKB, I/O
19	I/O	I/O
20	V_{CCA}	V_{CCA}
21	CLKA, I/O	CLKA, I/O
22	I/O	I/O
23	PRA, I/O	PRA, I/O
24	NC	WD, I/O
25	I/O	WD, I/O
26	I/O	I/O
27	I/O	I/O
28	NC	I/O
29	I/O	WD, I/O
30	GND	GND
31	NC	WD, I/O
32	I/O	I/O
33	I/O	I/O
34	I/O	I/O
35	NC	V_{CCI}

160-Pin PQFP		
Pin Number	**A42MX09 Function**	**A42MX24 Function**
36	I/O	WD, I/O
37	I/O	WD, I/O
38	SDI, I/O	SDI, I/O
39	I/O	I/O
40	GND	GND
41	I/O	I/O
42	I/O	I/O
43	I/O	I/O
44	GND	GND
45	I/O	I/O
46	I/O	I/O
47	I/O	I/O
48	I/O	I/O
49	GND	GND
50	I/O	I/O
51	I/O	I/O
52	NC	I/O
53	I/O	I/O
54	NC	V_{CCA}
55	I/O	I/O
56	I/O	I/O
57	V_{CCA}	V_{CCA}
58	V_{CCI}	V_{CCI}
59	GND	GND
60	V_{CCA}	V_{CCA}
61	GND	GND
62	I/O	TCK, I/O
63	I/O	I/O
64	GND	GND
65	I/O	I/O
66	I/O	I/O
67	I/O	I/O
68	I/O	I/O
69	GND	GND
70	NC	I/O

160-Pin PQFP		
Pin Number	**A42MX09 Function**	**A42MX24 Function**
71	I/O	I/O
72	I/O	I/O
73	I/O	I/O
74	I/O	I/O
75	NC	I/O
76	I/O	I/O
77	NC	I/O
78	I/O	I/O
79	NC	I/O
80	GND	GND
81	I/O	I/O
82	SDO, I/O	SDO, TDO, I/O
83	I/O	WD, I/O
84	I/O	WD, I/O
85	I/O	I/O
86	NC	V_{CCI}
87	I/O	I/O
88	I/O	WD, I/O
89	GND	GND
90	NC	I/O
91	I/O	I/O
92	I/O	I/O
93	I/O	I/O
94	I/O	I/O
95	I/O	I/O
96	I/O	WD, I/O
97	I/O	I/O
98	V_{CCA}	V_{CCA}
99	GND	GND
100	NC	I/O
101	I/O	I/O
102	I/O	I/O
103	NC	I/O
104	I/O	I/O
105	I/O	I/O

160-Pin PQFP		
Pin Number	**A42MX09 Function**	**A42MX24 Function**
106	I/O	WD, I/O
107	I/O	WD, I/O
108	I/O	I/O
109	GND	GND
110	NC	I/O
111	I/O	WD, I/O
112	I/O	WD, I/O
113	I/O	I/O
114	NC	V_{CCI}
115	I/O	WD, I/O
116	NC	WD, I/O
117	I/O	I/O
118	I/O	TDI, I/O
119	I/O	TMS, I/O
120	GND	GND
121	I/O	I/O
122	I/O	I/O
123	I/O	I/O
124	NC	I/O
125	GND	GND
126	I/O	I/O
127	I/O	I/O
128	I/O	I/O
129	NC	I/O
130	GND	GND
131	I/O	I/O
132	I/O	I/O
133	I/O	I/O
134	I/O	I/O
135	NC	V_{CCA}
136	I/O	I/O
137	I/O	I/O
138	NC	V_{CCA}
139	V_{CCI}	V_{CCI}
140	GND	GND

160-Pin PQFP		
Pin Number	**A42MX09 Function**	**A42MX24 Function**
141	NC	I/O
142	I/O	I/O
143	I/O	I/O
144	I/O	I/O
145	GND	GND
146	NC	I/O
147	I/O	I/O
148	I/O	I/O
149	I/O	I/O
150	NC	V_{CCA}
151	NC	I/O
152	NC	I/O
153	NC	I/O
154	NC	I/O
155	GND	GND
156	I/O	I/O
157	I/O	I/O
158	I/O	I/O
159	MODE	MODE
160	GND	GND

208-Pin PQFP Package (Top View)

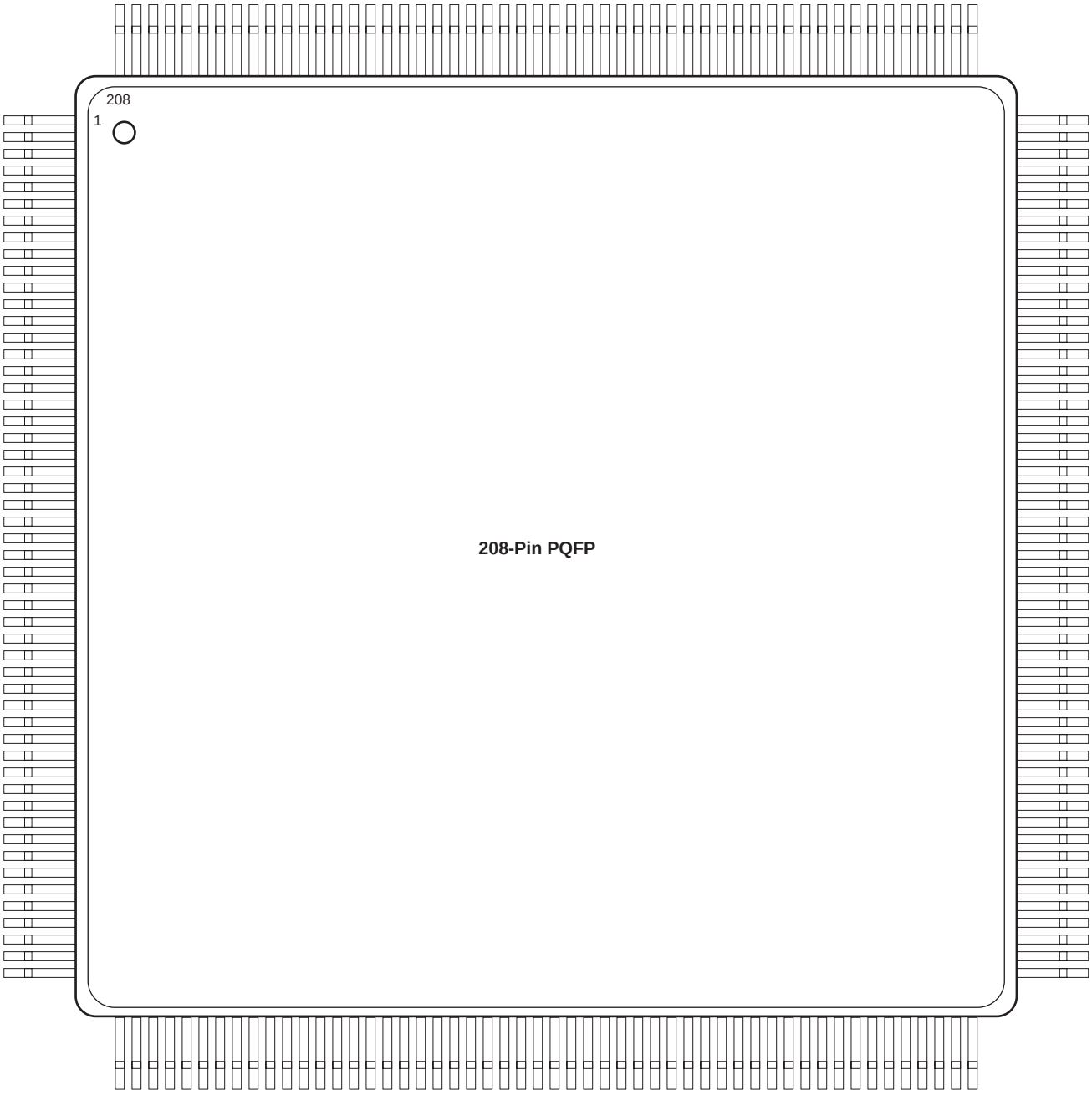


Figure 2-5 • **208-Pin PQFP**

208-Pin PQFP			
Pin Number	A42MX16 Function	A42MX24 Function	A42MX36 Function
1	GND	GND	GND
2	NC	V_{CCA}	V_{CCA}
3	MODE	MODE	MODE
4	I/O	I/O	I/O
5	I/O	I/O	I/O
6	I/O	I/O	I/O
7	I/O	I/O	I/O
8	I/O	I/O	I/O
9	NC	I/O	I/O
10	NC	I/O	I/O
11	NC	I/O	I/O
12	I/O	I/O	I/O
13	I/O	I/O	I/O
14	I/O	I/O	I/O
15	I/O	I/O	I/O
16	NC	I/O	I/O
17	V_{CCA}	V_{CCA}	V_{CCA}
18	I/O	I/O	I/O
19	I/O	I/O	I/O
20	I/O	I/O	I/O
21	I/O	I/O	I/O
22	GND	GND	GND
23	I/O	I/O	I/O
24	I/O	I/O	I/O
25	I/O	I/O	I/O
26	I/O	I/O	I/O
27	GND	GND	GND
28	V_{CCI}	V_{CCI}	V_{CCI}
29	V_{CCA}	V_{CCA}	V_{CCA}
30	I/O	I/O	I/O
31	I/O	I/O	I/O
32	V_{CCA}	V_{CCA}	V_{CCA}
33	I/O	I/O	I/O
34	I/O	I/O	I/O
35	I/O	I/O	I/O

208-Pin PQFP			
Pin Number	A42MX16 Function	A42MX24 Function	A42MX36 Function
36	I/O	I/O	I/O
37	I/O	I/O	I/O
38	I/O	I/O	I/O
39	I/O	I/O	I/O
40	I/O	I/O	I/O
41	NC	I/O	I/O
42	NC	I/O	I/O
43	NC	I/O	I/O
44	I/O	I/O	I/O
45	I/O	I/O	I/O
46	I/O	I/O	I/O
47	I/O	I/O	I/O
48	I/O	I/O	I/O
49	I/O	I/O	I/O
50	NC	I/O	I/O
51	NC	I/O	I/O
52	GND	GND	GND
53	GND	GND	GND
54	I/O	TMS, I/O	TMS, I/O
55	I/O	TDI, I/O	TDI, I/O
56	I/O	I/O	I/O
57	I/O	WD, I/O	WD, I/O
58	I/O	WD, I/O	WD, I/O
59	I/O	I/O	I/O
60	V_{CCI}	V_{CCI}	V_{CCI}
61	NC	I/O	I/O
62	NC	I/O	I/O
63	I/O	I/O	I/O
64	I/O	I/O	I/O
65	I/O	I/O	QCLKA, I/O
66	I/O	WD, I/O	WD, I/O
67	NC	WD, I/O	WD, I/O
68	NC	I/O	I/O
69	I/O	I/O	I/O
70	I/O	WD, I/O	WD, I/O

208-Pin PQFP			
Pin Number	**A42MX16 Function**	**A42MX24 Function**	**A42MX36 Function**
71	I/O	WD, I/O	WD, I/O
72	I/O	I/O	I/O
73	I/O	I/O	I/O
74	I/O	I/O	I/O
75	I/O	I/O	I/O
76	I/O	I/O	I/O
77	I/O	I/O	I/O
78	GND	GND	GND
79	V_{CCA}	V_{CCA}	V_{CCA}
80	NC	V_{CCI}	V_{CCI}
81	I/O	I/O	I/O
82	I/O	I/O	I/O
83	I/O	I/O	I/O
84	I/O	I/O	I/O
85	I/O	WD, I/O	WD, I/O
86	I/O	WD, I/O	WD, I/O
87	I/O	I/O	I/O
88	I/O	I/O	I/O
89	NC	I/O	I/O
90	NC	I/O	I/O
91	I/O	I/O	QCLKB, I/O
92	I/O	I/O	I/O
93	I/O	WD, I/O	WD, I/O
94	I/O	WD, I/O	WD, I/O
95	NC	I/O	I/O
96	NC	I/O	I/O
97	NC	I/O	I/O
98	V_{CCI}	V_{CCI}	V_{CCI}
99	I/O	I/O	I/O
100	I/O	WD, I/O	WD, I/O
101	I/O	WD, I/O	WD, I/O
102	I/O	I/O	I/O
103	SDO, I/O	SDO, TDO, I/O	SDO, TDO, I/O
104	I/O	I/O	I/O
105	GND	GND	GND

208-Pin PQFP			
Pin Number	**A42MX16 Function**	**A42MX24 Function**	**A42MX36 Function**
106	NC	V_{CCA}	V_{CCA}
107	I/O	I/O	I/O
108	I/O	I/O	I/O
109	I/O	I/O	I/O
110	I/O	I/O	I/O
111	I/O	I/O	I/O
112	NC	I/O	I/O
113	NC	I/O	I/O
114	NC	I/O	I/O
115	NC	I/O	I/O
116	I/O	I/O	I/O
117	I/O	I/O	I/O
118	I/O	I/O	I/O
119	I/O	I/O	I/O
120	I/O	I/O	I/O
121	I/O	I/O	I/O
122	I/O	I/O	I/O
123	I/O	I/O	I/O
124	I/O	I/O	I/O
125	I/O	I/O	I/O
126	GND	GND	GND
127	I/O	I/O	I/O
128	I/O	TCK, I/O	TCK, I/O
129	GND	GND	GND
130	V_{CCA}	V_{CCA}	V_{CCA}
131	GND	GND	GND
132	V_{CCI}	V_{CCI}	V_{CCI}
133	V_{CCA}	V_{CCA}	V_{CCA}
134	I/O	I/O	I/O
135	I/O	I/O	I/O
136	V_{CCA}	V_{CCA}	V_{CCA}
137	I/O	I/O	I/O
138	I/O	I/O	I/O
139	I/O	I/O	I/O
140	I/O	I/O	I/O

208-Pin PQFP			
Pin Number	A42MX16 Function	A42MX24 Function	A42MX36 Function
141	NC	I/O	I/O
142	I/O	I/O	I/O
143	I/O	I/O	I/O
144	I/O	I/O	I/O
145	I/O	I/O	I/O
146	NC	I/O	I/O
147	NC	I/O	I/O
148	NC	I/O	I/O
149	NC	I/O	I/O
150	GND	GND	GND
151	I/O	I/O	I/O
152	I/O	I/O	I/O
153	I/O	I/O	I/O
154	I/O	I/O	I/O
155	I/O	I/O	I/O
156	I/O	I/O	I/O
157	GND	GND	GND
158	I/O	I/O	I/O
159	SDI, I/O	SDI, I/O	SDI, I/O
160	I/O	I/O	I/O
161	I/O	WD, I/O	WD, I/O
162	I/O	WD, I/O	WD, I/O
163	I/O	I/O	I/O
164	V_{CCI}	V_{CCI}	V_{CCI}
165	NC	I/O	I/O
166	NC	I/O	I/O
167	I/O	I/O	I/O
168	I/O	WD, I/O	WD, I/O
169	I/O	WD, I/O	WD, I/O
170	I/O	I/O	I/O
171	NC	I/O	QCLKD, I/O
172	I/O	I/O	I/O
173	I/O	I/O	I/O
174	I/O	I/O	I/O
175	I/O	I/O	I/O

208-Pin PQFP			
Pin Number	A42MX16 Function	A42MX24 Function	A42MX36 Function
176	I/O	WD, I/O	WD, I/O
177	I/O	WD, I/O	WD, I/O
178	PRA, I/O	PRA, I/O	PRA, I/O
179	I/O	I/O	I/O
180	CLKA, I/O	CLKA, I/O	CLKA, I/O
181	NC	I/O	I/O
182	NC	V_{CCI}	V_{CCI}
183	V_{CCA}	V_{CCA}	V_{CCA}
184	GND	GND	GND
185	I/O	I/O	I/O
186	CLKB, I/O	CLKB, I/O	CLKB, I/O
187	I/O	I/O	I/O
188	PRB, I/O	PRB, I/O	PRB, I/O
189	I/O	I/O	I/O
190	I/O	WD, I/O	WD, I/O
191	I/O	WD, I/O	WD, I/O
192	I/O	I/O	I/O
193	NC	I/O	I/O
194	NC	WD, I/O	WD, I/O
195	NC	WD, I/O	WD, I/O
196	I/O	I/O	QCLKC, I/O
197	NC	I/O	I/O
198	I/O	I/O	I/O
199	I/O	I/O	I/O
200	I/O	I/O	I/O
201	NC	I/O	I/O
202	V_{CCI}	V_{CCI}	V_{CCI}
203	I/O	WD, I/O	WD, I/O
204	I/O	WD, I/O	WD, I/O
205	I/O	I/O	I/O
206	I/O	I/O	I/O
207	DCLK, I/O	DCLK, I/O	DCLK, I/O
208	I/O	I/O	I/O

240-Pin PQFP Package (Top View)

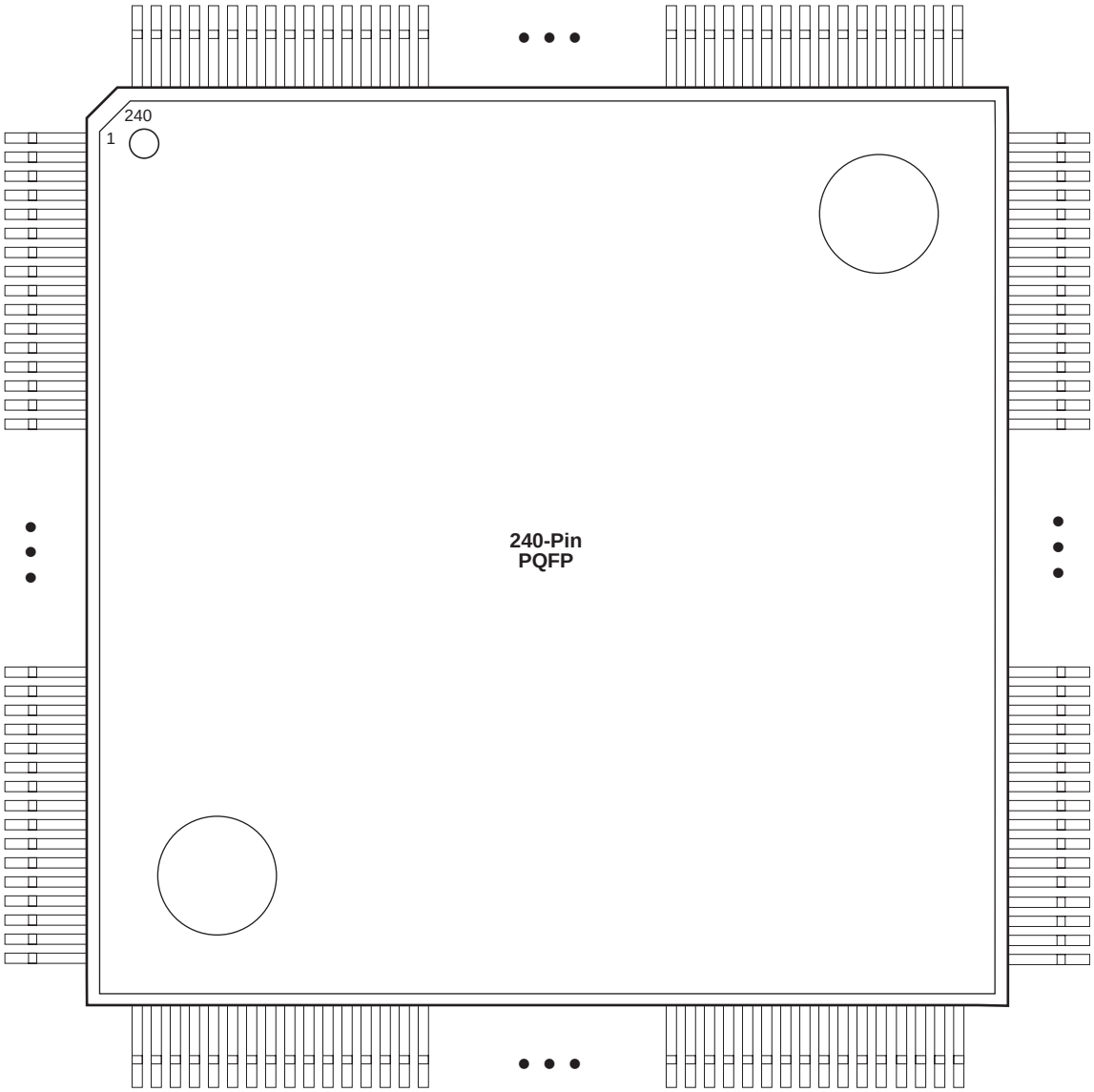


Figure 2-6 • **240-Pin PQFP**

240-Pin PQFP	
Pin Number	A42MX36 Function
1	I/O
2	DCLK, I/O
3	I/O
4	I/O
5	I/O
6	WD, I/O
7	WD, I/O
8	V_{CCI}
9	I/O
10	I/O
11	I/O
12	I/O
13	I/O
14	I/O
15	QCLKC, I/O
16	I/O
17	WD, I/O
18	WD, I/O
19	I/O
20	I/O
21	WD, I/O
22	WD, I/O
23	I/O
24	PRB, I/O
25	I/O
26	CLKB, I/O
27	I/O
28	GND
29	V_{CCA}
30	V_{CCI}
31	I/O
32	CLKA, I/O
33	I/O
34	PRA, I/O
35	I/O

240-Pin PQFP	
Pin Number	A42MX36 Function
36	I/O
37	WD, I/O
38	WD, I/O
39	I/O
40	I/O
41	I/O
42	I/O
43	I/O
44	I/O
45	QCLKD, I/O
46	I/O
47	WD, I/O
48	WD, I/O
49	I/O
50	I/O
51	I/O
52	V_{CCI}
53	I/O
54	WD, I/O
55	WD, I/O
56	I/O
57	SDI, I/O
58	I/O
59	V_{CCA}
60	GND
61	GND
62	I/O
63	I/O
64	I/O
65	I/O
66	I/O
67	I/O
68	I/O
69	I/O
70	I/O

240-Pin PQFP	
Pin Number	A42MX36 Function
71	V_{CCI}
72	I/O
73	I/O
74	I/O
75	I/O
76	I/O
77	I/O
78	I/O
79	I/O
80	I/O
81	I/O
82	I/O
83	I/O
84	I/O
85	V_{CCA}
86	I/O
87	I/O
88	V_{CCA}
89	V_{CCI}
90	V_{CCA}
91	GND
92	TCK, I/O
93	I/O
94	GND
95	I/O
96	I/O
97	I/O
98	I/O
99	I/O
100	I/O
101	I/O
102	I/O
103	I/O
104	I/O
105	I/O

240-Pin PQFP	
Pin Number	A42MX36 Function
106	I/O
107	I/O
108	V_{CCI}
109	I/O
110	I/O
111	I/O
112	I/O
113	I/O
114	I/O
115	I/O
116	I/O
117	I/O
118	V_{CCA}
119	GND
120	GND
121	GND
122	I/O
123	SDO, TDO, I/O
124	I/O
125	WD, I/O
126	WD, I/O
127	I/O
128	V_{CCI}
129	I/O
130	I/O
131	I/O
132	WD, I/O
133	WD, I/O
134	I/O
135	QCLKB, I/O
136	I/O
137	I/O
138	I/O
139	I/O
140	I/O

240-Pin PQFP	
Pin Number	A42MX36 Function
141	I/O
142	WD, I/O
143	WD, I/O
144	I/O
145	I/O
146	I/O
147	I/O
148	I/O
149	I/O
150	V_{CCI}
151	V_{CCA}
152	GND
153	I/O
154	I/O
155	I/O
156	I/O
157	I/O
158	I/O
159	WD, I/O
160	WD, I/O
161	I/O
162	I/O
163	WD, I/O
164	WD, I/O
165	I/O
166	QCLKA, I/O
167	I/O
168	I/O
169	I/O
170	I/O
171	I/O
172	V_{CCI}
173	I/O
174	WD, I/O
175	WD, I/O

240-Pin PQFP	
Pin Number	A42MX36 Function
176	I/O
177	I/O
178	TDI, I/O
179	TMS, I/O
180	GND
181	V_{CCA}
182	GND
183	I/O
184	I/O
185	I/O
186	I/O
187	I/O
188	I/O
189	I/O
190	I/O
191	I/O
192	V_{CCI}
193	I/O
194	I/O
195	I/O
196	I/O
197	I/O
198	I/O
199	I/O
200	I/O
201	I/O
202	I/O
203	I/O
204	I/O
205	I/O
206	V_{CCA}
207	I/O
208	I/O
209	V_{CCA}
210	V_{CCI}

240-Pin PQFP	
Pin Number	A42MX36 Function
211	I/O
212	I/O
213	I/O
214	I/O
215	I/O
216	I/O
217	I/O
218	I/O
219	V_{CCA}
220	I/O
221	I/O
222	I/O
223	I/O
224	I/O
225	I/O
226	I/O
227	V_{CCI}
228	I/O
229	I/O
230	I/O
231	I/O
232	I/O
233	I/O
234	I/O
235	I/O
236	I/O
237	GND
238	MODE
239	V_{CCA}
240	GND

80-Pin VQFP

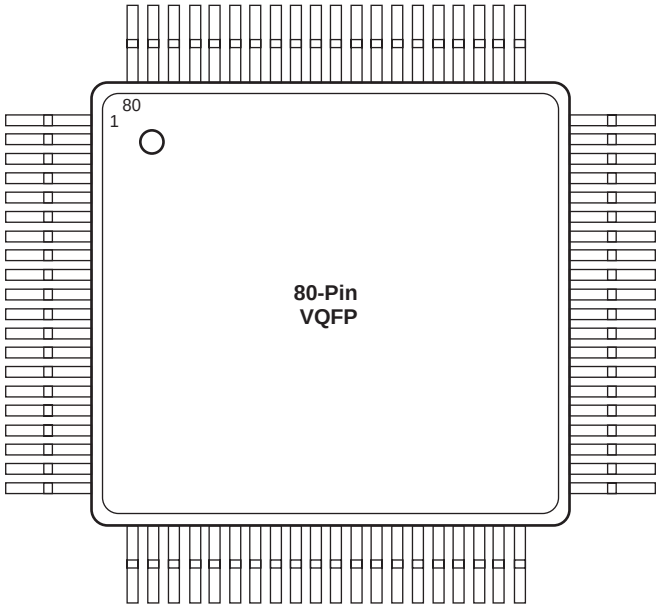


Figure 2-7 • **80-Pin VQFP**

80-Pin VQFP		
Pin Number	**A40MX02 Function**	**A40MX04 Function**
1	I/O	I/O
2	NC	I/O
3	NC	I/O
4	NC	I/O
5	I/O	I/O
6	I/O	I/O
7	GND	GND
8	I/O	I/O
9	I/O	I/O
10	I/O	I/O
11	I/O	I/O
12	I/O	I/O
13	V_{CC}	V_{CC}
14	I/O	I/O
15	I/O	I/O
16	I/O	I/O
17	NC	I/O
18	NC	I/O
19	NC	I/O
20	V_{CC}	V_{CC}
21	I/O	I/O
22	I/O	I/O
23	I/O	I/O
24	I/O	I/O
25	I/O	I/O
26	I/O	I/O
27	GND	GND
28	I/O	I/O
29	I/O	I/O
30	I/O	I/O
31	I/O	I/O
32	I/O	I/O
33	V_{CC}	V_{CC}
34	I/O	I/O
35	I/O	I/O
36	I/O	I/O
37	I/O	I/O
38	I/O	I/O
39	I/O	I/O
40	I/O	I/O

80-Pin VQFP		
Pin Number	**A40MX02 Function**	**A40MX04 Function**
41	NC	I/O
42	NC	I/O
43	NC	I/O
44	I/O	I/O
45	I/O	I/O
46	I/O	I/O
47	GND	GND
48	I/O	I/O
49	I/O	I/O
50	CLK, I/O	CLK, I/O
51	I/O	I/O
52	MODE	MODE
53	V_{CC}	V_{CC}
54	NC	I/O
55	NC	I/O
56	NC	I/O
57	SDI, I/O	SDI, I/O
58	DCLK, I/O	DCLK, I/O
59	PRA, I/O	PRA, I/O
60	NC	NC
61	PRB, I/O	PRB, I/O
62	I/O	I/O
63	I/O	I/O
64	I/O	I/O
65	I/O	I/O
66	I/O	I/O
67	I/O	I/O
68	GND	GND
69	I/O	I/O
70	I/O	I/O
71	I/O	I/O
72	I/O	I/O
73	I/O	I/O
74	V_{CC}	V_{CC}
75	I/O	I/O
76	I/O	I/O
77	I/O	I/O
78	I/O	I/O
79	I/O	I/O
80	I/O	I/O

100-Pin VQFP Package (Top View)

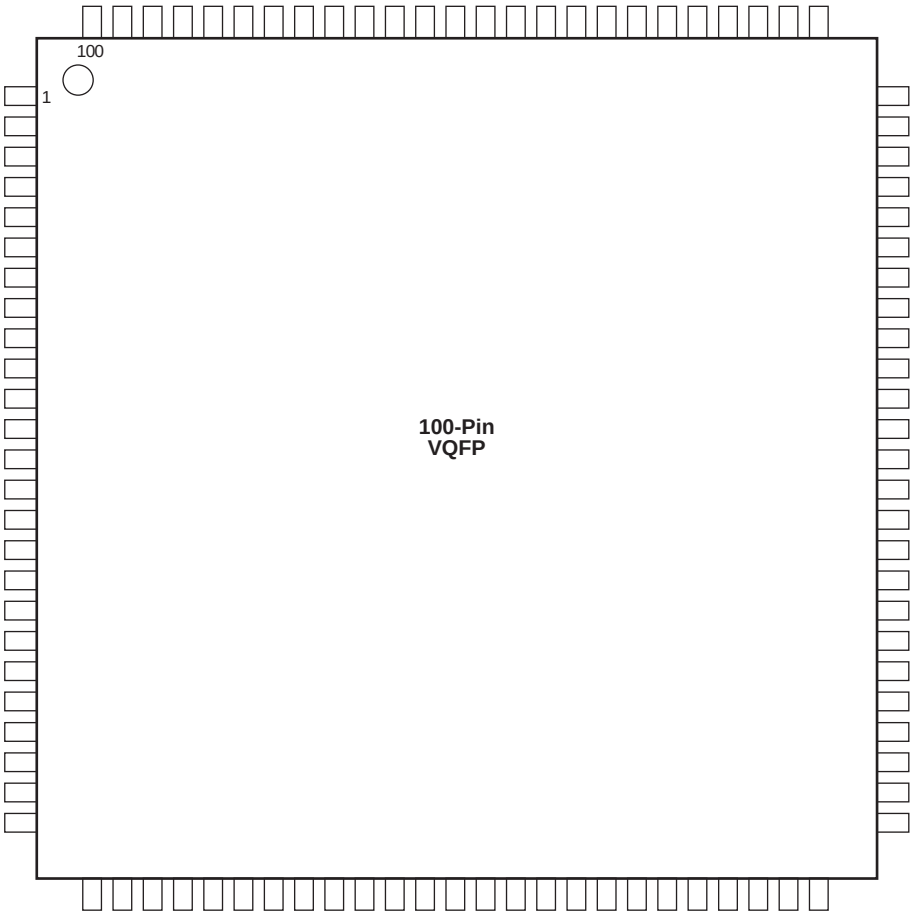


Figure 2-8 • **100-Pin VQFP**

100-Pin VQFP		
Pin Number	**A42MX09 Function**	**A42MX16 Function**
1	I/O	I/O
2	MODE	MODE
3	I/O	I/O
4	I/O	I/O
5	I/O	I/O
6	I/O	I/O
7	GND	GND
8	I/O	I/O
9	I/O	I/O
10	I/O	I/O
11	I/O	I/O
12	I/O	I/O
13	I/O	I/O
14	V_{CCA}	NC
15	V_{CCI}	V_{CCI}
16	I/O	I/O
17	I/O	I/O
18	I/O	I/O
19	I/O	I/O
20	GND	GND
21	I/O	I/O
22	I/O	I/O
23	I/O	I/O
24	I/O	I/O
25	I/O	I/O
26	I/O	I/O
27	I/O	I/O
28	I/O	I/O
29	I/O	I/O
30	I/O	I/O
31	I/O	I/O
32	GND	GND
33	I/O	I/O
34	I/O	I/O
35	I/O	I/O

100-Pin VQFP		
Pin Number	**A42MX09 Function**	**A42MX16 Function**
36	I/O	I/O
37	I/O	I/O
38	V_{CCA}	V_{CCA}
39	I/O	I/O
40	I/O	I/O
41	I/O	I/O
42	I/O	I/O
43	I/O	I/O
44	GND	GND
45	I/O	I/O
46	I/O	I/O
47	I/O	I/O
48	I/O	I/O
49	I/O	I/O
50	SDO, I/O	SDO, I/O
51	I/O	I/O
52	I/O	I/O
53	I/O	I/O
54	I/O	I/O
55	GND	GND
56	I/O	I/O
57	I/O	I/O
58	I/O	I/O
59	I/O	I/O
60	I/O	I/O
61	I/O	I/O
62	GND	GND
63	V_{CCA}	V_{CCA}
64	V_{CCI}	V_{CCI}
65	V_{CCA}	V_{CCA}
66	I/O	I/O
67	I/O	I/O
68	I/O	I/O
69	I/O	I/O
70	GND	GND

100-Pin VQFP		
Pin Number	**A42MX09 Function**	**A42MX16 Function**
71	I/O	I/O
72	I/O	I/O
73	I/O	I/O
74	I/O	I/O
75	I/O	I/O
76	I/O	I/O
77	SDI, I/O	SDI, I/O
78	I/O	I/O
79	I/O	I/O
80	I/O	I/O
81	I/O	I/O
82	GND	GND
83	I/O	I/O
84	I/O	I/O
85	PRA, I/O	PRA, I/O
86	I/O	I/O
87	CLKA, I/O	CLKA, I/O
88	V_{CCA}	V_{CCA}
89	I/O	I/O
90	CLKB, I/O	CLKB, I/O
91	I/O	I/O
92	PRB, I/O	PRB, I/O
93	I/O	I/O
94	GND	GND
95	I/O	I/O
96	I/O	I/O
97	I/O	I/O
98	I/O	I/O
99	I/O	I/O
100	DCLK, I/O	DCLK, I/O

176-Pin TQFP Package (Top View)

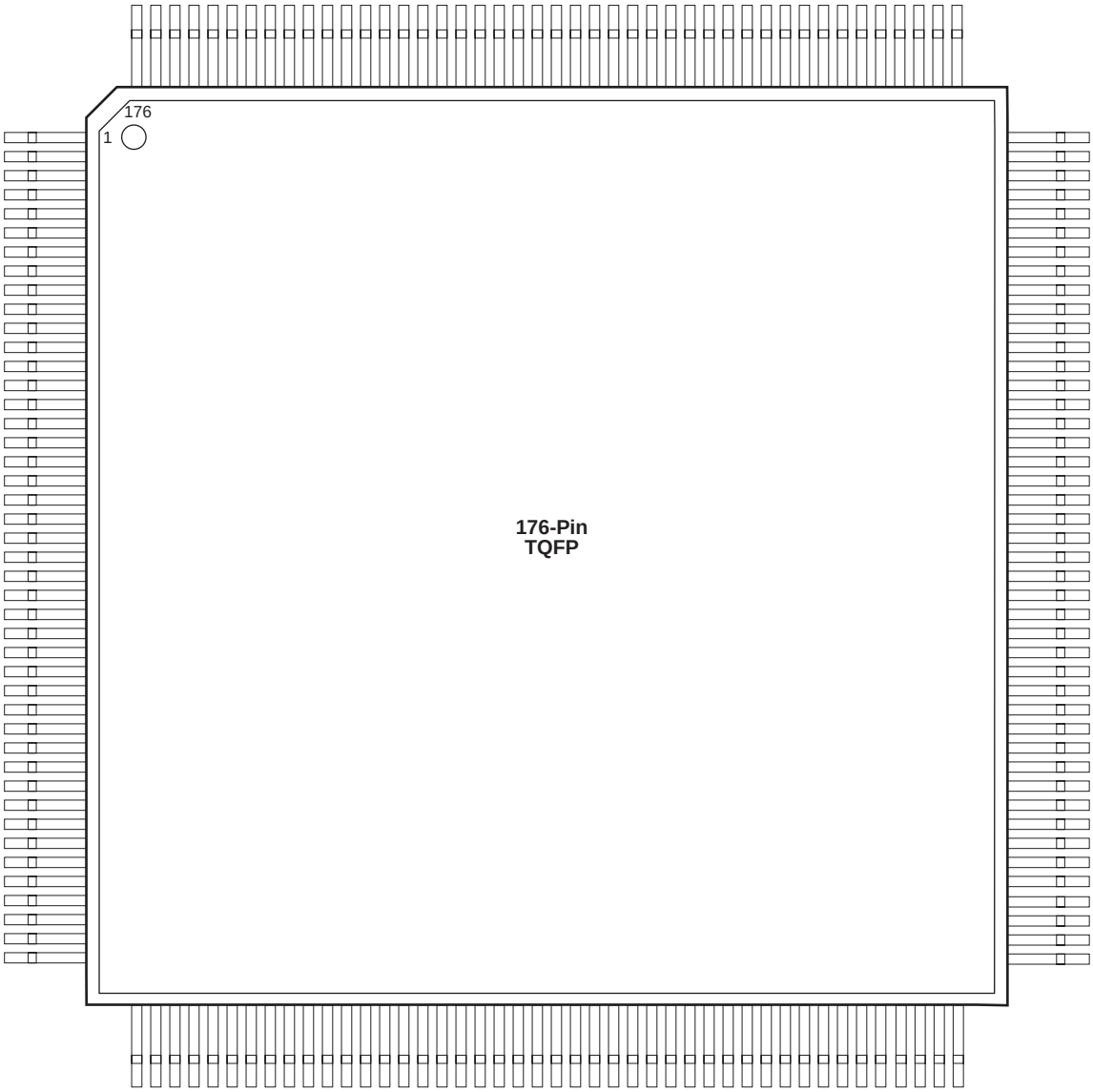


Figure 2-9 • **176-Pin TQFP**

176-Pin TQFP			
Pin Number	**A42MX09 Function**	**A42MX16 Function**	**A42MX24 Function**
1	GND	GND	GND
2	MODE	MODE	MODE
3	I/O	I/O	I/O
4	I/O	I/O	I/O
5	I/O	I/O	I/O
6	I/O	I/O	I/O
7	I/O	I/O	I/O
8	NC	NC	I/O
9	I/O	I/O	I/O
10	NC	I/O	I/O
11	NC	I/O	I/O
12	I/O	I/O	I/O
13	NC	V_{CCA}	V_{CCA}
14	I/O	I/O	I/O
15	I/O	I/O	I/O
16	I/O	I/O	I/O
17	I/O	I/O	I/O
18	GND	GND	GND
19	NC	I/O	I/O
20	NC	I/O	I/O
21	I/O	I/O	I/O
22	NC	I/O	I/O
23	GND	GND	GND
24	NC	V_{CCI}	V_{CCI}
25	V_{CCA}	V_{CCA}	V_{CCA}
26	NC	I/O	I/O
27	NC	I/O	I/O
28	V_{CCI}	V_{CCA}	V_{CCA}
29	NC	I/O	I/O
30	I/O	I/O	I/O
31	I/O	I/O	I/O
32	I/O	I/O	I/O
33	NC	NC	I/O
34	I/O	I/O	I/O
35	I/O	I/O	I/O
36	I/O	I/O	I/O
37	NC	I/O	I/O

176-Pin TQFP			
Pin Number	**A42MX09 Function**	**A42MX16 Function**	**A42MX24 Function**
38	NC	NC	I/O
39	I/O	I/O	I/O
40	I/O	I/O	I/O
41	I/O	I/O	I/O
42	I/O	I/O	I/O
43	I/O	I/O	I/O
44	I/O	I/O	I/O
45	GND	GND	GND
46	I/O	I/O	TMS, I/O
47	I/O	I/O	TDI, I/O
48	I/O	I/O	I/O
49	I/O	I/O	WD, I/O
50	I/O	I/O	WD, I/O
51	I/O	I/O	I/O
52	NC	V_{CCI}	V_{CCI}
53	I/O	I/O	I/O
54	NC	I/O	I/O
55	NC	I/O	WD, I/O
56	I/O	I/O	WD, I/O
57	NC	NC	I/O
58	I/O	I/O	I/O
59	I/O	I/O	WD, I/O
60	I/O	I/O	WD, I/O
61	NC	I/O	I/O
62	I/O	I/O	I/O
63	I/O	I/O	I/O
64	NC	I/O	I/O
65	I/O	I/O	I/O
66	NC	I/O	I/O
67	GND	GND	GND
68	V_{CCA}	V_{CCA}	V_{CCA}
69	I/O	I/O	WD, I/O
70	I/O	I/O	WD, I/O
71	I/O	I/O	I/O
72	I/O	I/O	I/O
73	I/O	I/O	I/O
74	NC	I/O	I/O

176-Pin TQFP			
Pin Number	**A42MX09 Function**	**A42MX16 Function**	**A42MX24 Function**
75	I/O	I/O	I/O
76	I/O	I/O	I/O
77	NC	NC	WD, I/O
78	NC	I/O	WD, I/O
79	I/O	I/O	I/O
80	NC	I/O	I/O
81	I/O	I/O	I/O
82	NC	V_{CCI}	V_{CCI}
83	I/O	I/O	I/O
84	I/O	I/O	WD, I/O
85	I/O	I/O	WD, I/O
86	NC	I/O	I/O
87	SDO, I/O	SDO, I/O	SDO, TDO, I/O
88	I/O	I/O	I/O
89	GND	GND	GND
90	I/O	I/O	I/O
91	I/O	I/O	I/O
92	I/O	I/O	I/O
93	I/O	I/O	I/O
94	I/O	I/O	I/O
95	I/O	I/O	I/O
96	NC	I/O	I/O
97	NC	I/O	I/O
98	I/O	I/O	I/O
99	I/O	I/O	I/O
100	I/O	I/O	I/O
101	NC	NC	I/O
102	I/O	I/O	I/O
103	NC	I/O	I/O
104	I/O	I/O	I/O
105	I/O	I/O	I/O
106	GND	GND	GND
107	NC	I/O	I/O
108	NC	I/O	TCK, I/O
109	GND	GND	GND
110	V_{CCA}	V_{CCA}	V_{CCA}
111	GND	GND	GND

176-Pin TQFP			
Pin Number	**A42MX09 Function**	**A42MX16 Function**	**A42MX24 Function**
112	V_{CCI}	V_{CCI}	V_{CCI}
113	V_{CCA}	V_{CCA}	V_{CCA}
114	NC	I/O	I/O
115	NC	I/O	I/O
116	NC	V_{CCA}	V_{CCA}
117	I/O	I/O	I/O
118	I/O	I/O	I/O
119	I/O	I/O	I/O
120	I/O	I/O	I/O
121	NC	NC	I/O
122	I/O	I/O	I/O
123	I/O	I/O	I/O
124	NC	I/O	I/O
125	NC	I/O	I/O
126	NC	NC	I/O
127	I/O	I/O	I/O
128	I/O	I/O	I/O
129	I/O	I/O	I/O
130	I/O	I/O	I/O
131	I/O	I/O	I/O
132	I/O	I/O	I/O
133	GND	GND	GND
134	I/O	I/O	I/O
135	SDI, I/O	SDI, I/O	SDI, I/O
136	NC	I/O	I/O
137	I/O	I/O	WD, I/O
138	I/O	I/O	WD, I/O
139	I/O	I/O	I/O
140	NC	V_{CCI}	V_{CCI}
141	I/O	I/O	I/O
142	I/O	I/O	I/O
143	NC	I/O	I/O
144	NC	I/O	WD, I/O
145	NC	NC	WD, I/O
146	I/O	I/O	I/O
147	NC	I/O	I/O
148	I/O	I/O	I/O

176-Pin TQFP			
Pin Number	**A42MX09 Function**	**A42MX16 Function**	**A42MX24 Function**
149	I/O	I/O	I/O
150	I/O	I/O	WD, I/O
151	NC	I/O	WD, I/O
152	PRA, I/O	PRA, I/O	PRA, I/O
153	I/O	I/O	I/O
154	CLKA, I/O	CLKA, I/O	CLKA, I/O
155	V_{CCA}	V_{CCA}	V_{CCA}
156	GND	GND	GND
157	I/O	I/O	I/O
158	CLKB, I/O	CLKB, I/O	CLKB, I/O
159	I/O	I/O	I/O
160	PRB, I/O	PRB, I/O	PRB, I/O
161	NC	I/O	WD, I/O
162	I/O	I/O	WD, I/O
163	I/O	I/O	I/O
164	I/O	I/O	I/O
165	NC	NC	WD, I/O
166	NC	I/O	WD, I/O
167	I/O	I/O	I/O
168	NC	I/O	I/O
169	I/O	I/O	I/O
170	NC	V_{CCI}	V_{CCI}
171	I/O	I/O	WD, I/O
172	I/O	I/O	WD, I/O
173	NC	I/O	I/O
174	I/O	I/O	I/O
175	DCLK, I/O	DCLK, I/O	DCLK, I/O
176	I/O	I/O	I/O

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In order to provide the latest information to designers, some datasheets are published before data has been fully characterized. Datasheets are designated as "Product Brief," "Advanced," "Production," and "Datasheet Supplement." The definition of these categories are as follows:

Product Brief

The product brief is a summarized version of a datasheet (advanced or production) containing general product information. This brief gives an overview of specific device and family information.

Advanced

This datasheet version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production.

Unmarked (production)

This datasheet version contains information that is considered to be final.

Datasheet Supplement

The datasheet supplement gives specific device information for a derivative family that differs from the general family datasheet. The supplement is to be used in conjunction with the datasheet to obtain more detailed information and for specifications that do not differ between the two families.

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